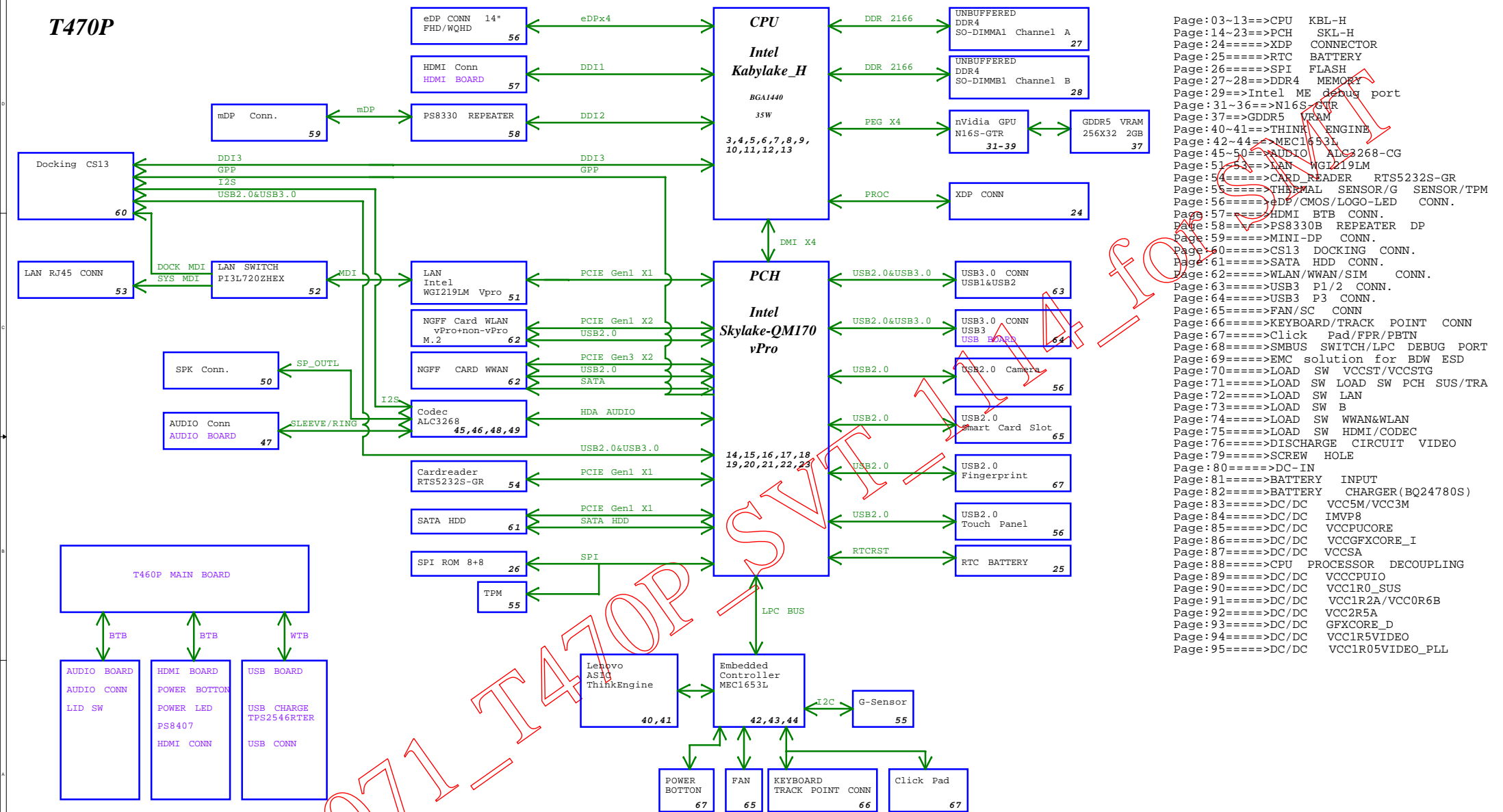


T470P



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Page: 14-23==>PCH SKL-H
Page: 24=====>XDP CONNECTOR
Page: 25=====>RTC BATTERY
Page: 26=====>SPI FLASH
Page: 27-28==>DDR4 MEMORY
Page: 29==>Intel ME debug port
Page: 31-36==>N16S-CUR
Page: 37==>GDDR5 VRAM
Page: 40-41==>THINK ENGINE
Page: 42-44==>MEC16531
Page: 45-50==>AUDIO1 ALC3268-CG
Page: 51-53==>LAN WGI2191M
Page: 54=====>CARD READER RTS5232S-GR
Page: 55=====>THERMAL SENSOR/G SENSOR/TPM
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Page: 83=====>DC/DC VCC5M/VCC3M
Page: 84=====>DC/DC IMVP8
Page: 85=====>DC/DC VCCPUCORE
Page: 86=====>DC/DC VCCGFXCORE_I
Page: 87=====>DC/DC VCCSA
Page: 88=====>CPU PROCESSOR DECOUPLING
Page: 89=====>DC/DC VCCCPUIO
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Page: 91=====>DC/DC VCC1R2A/VCCOR6B
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Page: 93=====>DC/DC GFXCORE_D
Page: 94=====>DC/DC VCC1R5VIDEO
Page: 95=====>DC/DC VCC1R05VIDEO_PLL

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			Wednesday, October 12, 2016 Sheet 1 of 0

TABLE: SYSTEM POWER STATE

Gx State (System State)	Sx State (System State)	Mx State (System State)	SW Power	M Power	SUS Power	AMT Power	A Power	B Power	User Observation	Chipset
G0	S0	M0	ON	ON	ON	ON	ON	ON	System Operating	Full On
G1	S3	M3	ON	ON	ON	ON	ON	OFF	Standby	Suspend-to-RAM (STR)
		M-OFF	ON	ON	ON	OFF	ON	OFF	Standby with USB wake enabled	
	Deep S3	M-OFF	ON	ON	OFF	OFF	ON	OFF	Standby	Suspend-to-Disk (STD)
	S4	M3	ON	ON	ON	ON	OFF	OFF	Hibernation with RTC wakeup	
	Deep S4	M-OFF	ON	ON	OFF	OFF	ON	OFF		
G2	S5	M3	ON	ON	ON	ON	OFF	OFF	Hibernation or Shutdown	Soft Off
	Deep S5	M-OFF	ON	ON	OFF	OFF	ON	OFF		
	S5 EC OFF	M-OFF	ON	OFF	OFF	OFF	OFF	OFF		
G3	---	---	OFF	OFF	OFF	OFF	OFF	OFF	No Power	Mechanical Off

Schematics Mark Definition

Capacitor Naming Note

Ceramic Capacitors:

0.1U_0402_6.3VXX

Tolerance
Temperature Characteristics
Rated Voltage
Package Size

Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7	8	9	A
Code	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R	NPO	COG	X6S

B	C	D	E	F	G	H	I	J	K	L
BJ	CH	CJ	CK	SH	SJ	UJ	UK	SK	X5S	NOJ

Tolerance:

Symbol	A	B	C	D	F	G	H	J	K	M	N
Tolerance	+0.05PF	+0.1PF	+0.25PF	+0.5PF	+1%	+2%	+3%	+5%	+10%	+20%	+30%

Symbol	P	Q	V	X	Z	S	Y
Tolerance	+100,-0%	+30,-10%	+20,-10%	+40,-20%	+80,-20%	+50,-20%	-30% ~ 10%

EC SMBus0 address

Device	Address
Smart Battery	0001 011X b

EC SMBus1 address

Device	Address
G-Sensor (LS3DH)	0011 000Xb
G-Sensor (KX023)	0011 110Xb

EC SMBus2 address

Device	Address
Charge Controller	0001 0010

EC SMBus10 address

Device	Address
Master VGA	0x9E

PCH SM Bus address

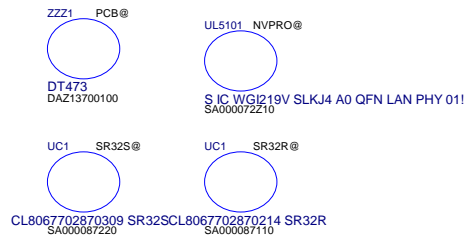
Device	Address
CH-A DDR DMM1	1001 0000b
CH-B DDR DMM2	1001 0010b

PCH SM Bus0 address



Device	Address
Intel Lan_I219	0XC8



BOM Structure Table

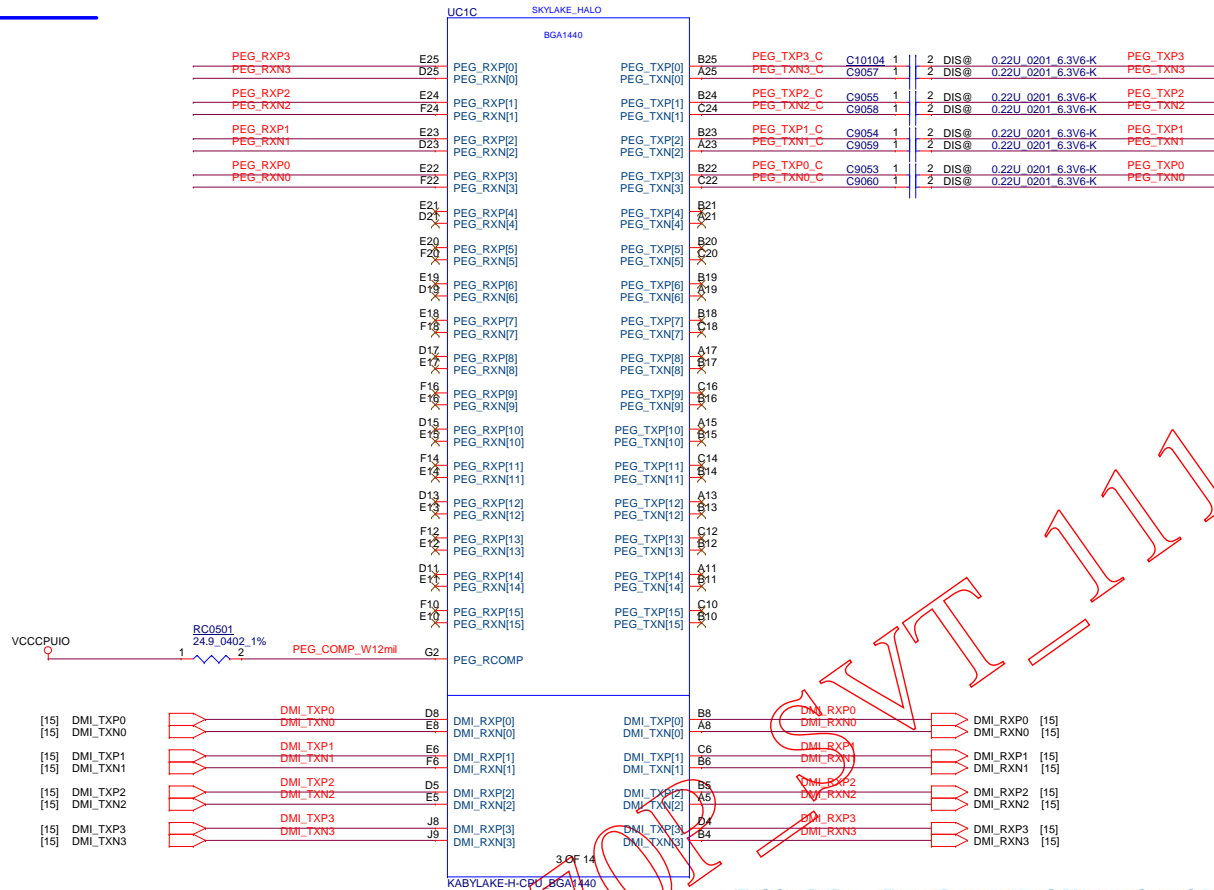
BOM Structure	NOTE
DEBUG@	For EE DEBUG
DPRE@	DP re-driver function
NODPRE@	Disable DP re-driver
GC6@	For GC6 function
NGC6@	NON GC6 function
ME@	ME Connector
EMC@	For EMI Solution
RF@	For RF Solution
VSE2G@	For SAMSUNG VRAM Setting
VME2G@	For Micron VRAM Setting
VHC2G@	For RF HYNIX VRAM Setting
X76_VSE2G@	K4W4G1646E-BC1A x4 + 24.9K
X76_VME2G@	MT41J256M16HA-093G x4 +10k
X76_VHC2G@	H5TC4G63CFR-N0C x4 +30.1k
CS@	For CURRENT SENSE
UMA@	For UMA
DIS@	For DIS
UC1@	For CPU



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Date: Wednesday, November 09, 2016				Rev 0.2 Sheet 2 of 99

[31] PEG_RXP[3:0] 
[31] PEG_RXN[3:0] 

 PEG_TXP[3:0] [31]
 PEG_TXN[3:0] [31]




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Table 8-3. Few Supported Normal and Lane-reversed Bifurcation Configurations

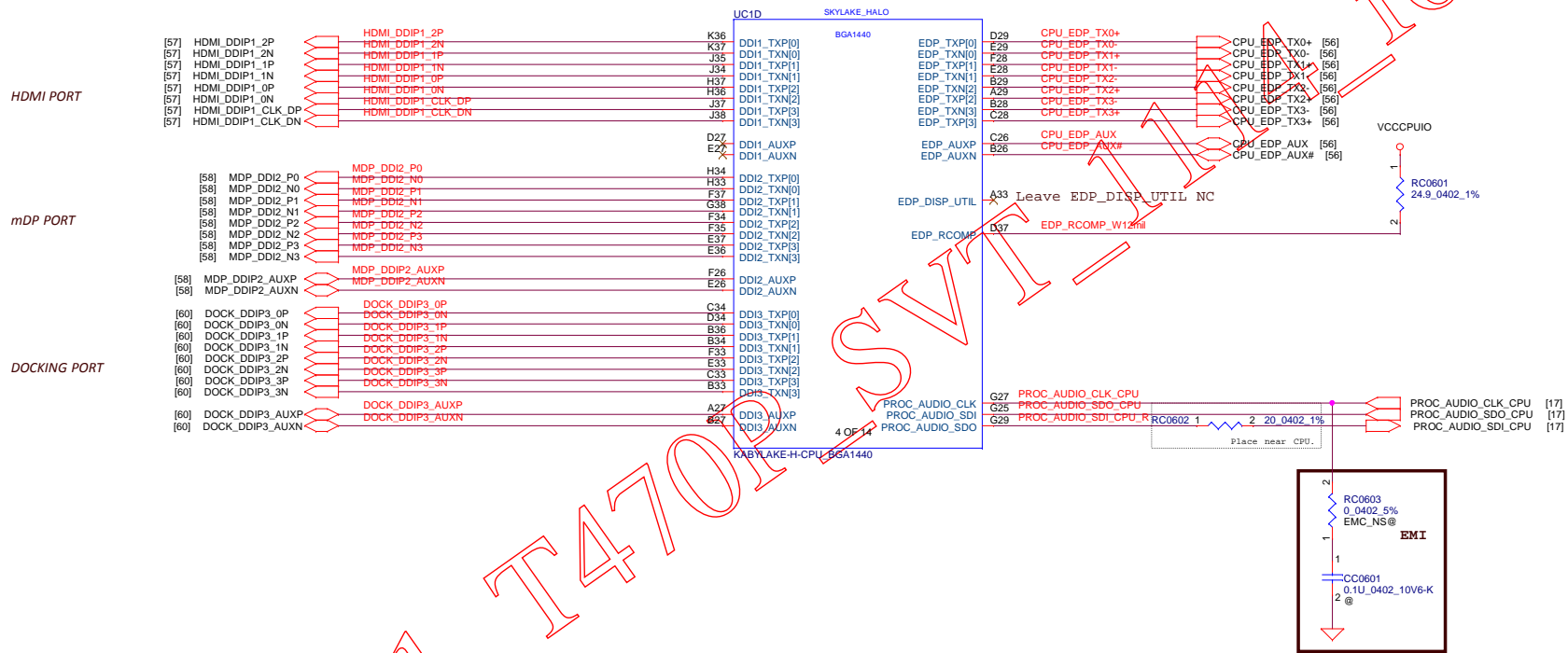
x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Pro- cessor	Physical Lanes															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0


Notes:

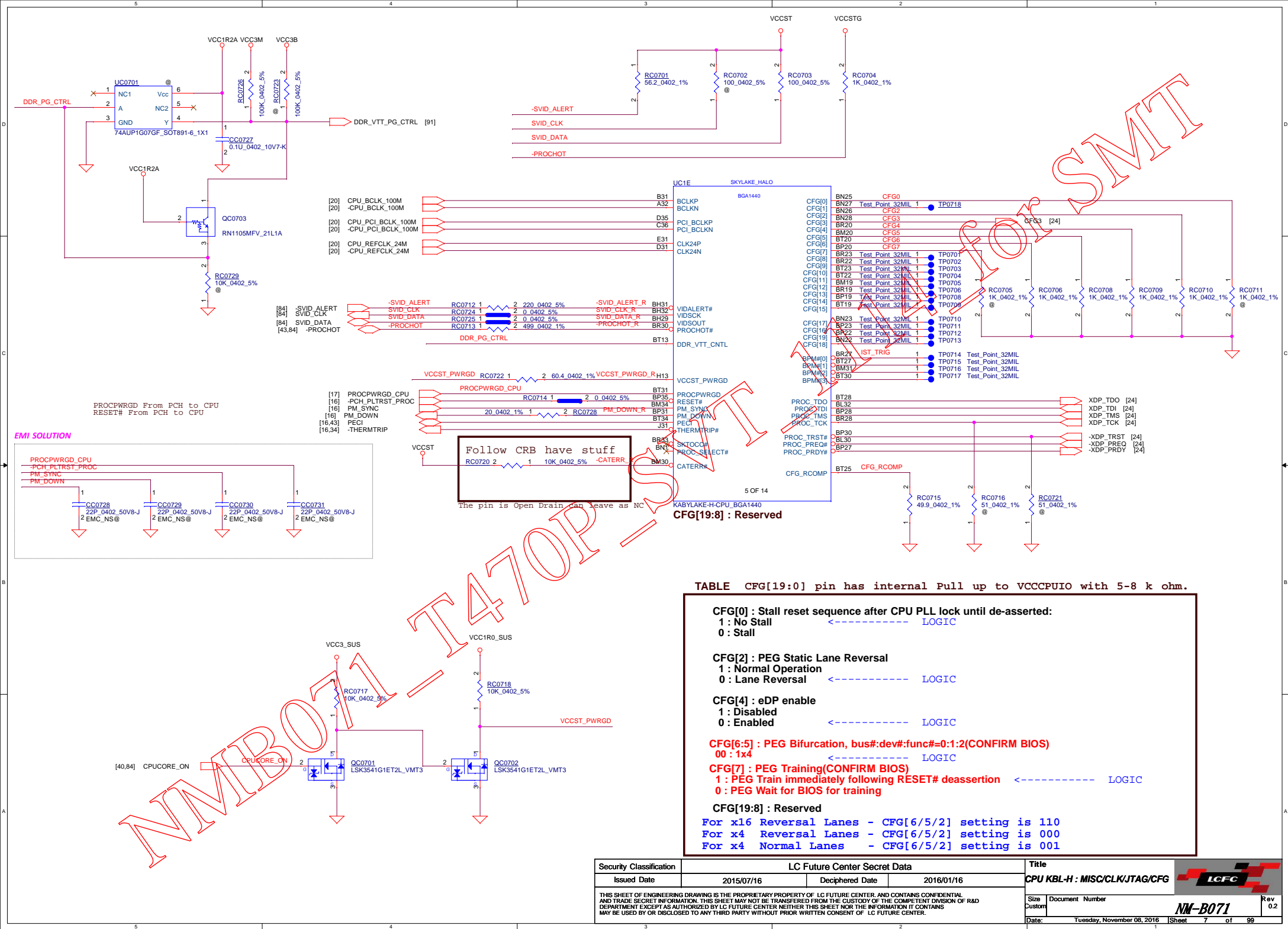
- Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
- In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
 - Connect lane 0 of 1st device to lane 0.
 - Connect lane 0 of 2nd device to lane 8.
 - Connect lane 0 of 3rd device to lane 12.For example:
 - When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
 - When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
 - When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9, one lane device must use lane 12.

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NMB071-T470P2-SVT for SMT



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NMIBO71-470P

UC1F SKYLAKE_HALO		
BGA1440		
Y38	VSS_1	VSS_78
Y37	VSS_2	VSS_79
Y14	VSS_3	VSS_80
Y13	VSS_4	VSS_81
Y11	VSS_5	VSS_82
Y10	VSS_6	VSS_83
Y9	VSS_7	VSS_84
Y8	VSS_8	VSS_85
Y7	VSS_9	VSS_86
W34	VSS_10	VSS_87
W33	VSS_11	VSS_88
W12	VSS_12	VSS_89
W5	VSS_13	VSS_90
W4	VSS_14	VSS_91
W3	VSS_15	VSS_92
W2	VSS_16	VSS_93
W1	VSS_17	VSS_94
V30	VSS_18	VSS_95
V29	VSS_19	VSS_96
V12	VSS_20	VSS_97
V6	VSS_21	VSS_98
U38	VSS_22	VSS_99
U37	VSS_23	VSS_100
U6	VSS_24	VSS_101
T34	VSS_25	VSS_102
T33	VSS_26	VSS_103
T14	VSS_27	VSS_104
T13	VSS_28	VSS_105
T12	VSS_29	VSS_106
T11	VSS_30	VSS_107
T9	VSS_31	VSS_108
T8	VSS_32	VSS_109
T7	VSS_33	VSS_110
T5	VSS_34	VSS_111
T4	VSS_35	VSS_112
T3	VSS_36	VSS_113
T2	VSS_37	VSS_114
T1	VSS_38	VSS_115
R30	VSS_39	VSS_116
R29	VSS_40	VSS_117
R12	VSS_41	VSS_118
P38	VSS_42	VSS_119
P37	VSS_43	VSS_120
P12	VSS_44	VSS_121
P6	VSS_45	VSS_122
N34	VSS_46	VSS_123
N33	VSS_47	VSS_124
N12	VSS_48	VSS_125
N11	VSS_49	VSS_126
N10	VSS_50	VSS_127
N9	VSS_51	VSS_128
N8	VSS_52	VSS_129
N7	VSS_53	VSS_130
N6	VSS_54	VSS_131
N5	VSS_55	VSS_132
N4	VSS_56	VSS_133
N3	VSS_57	VSS_134
N2	VSS_58	VSS_135
N1	VSS_59	VSS_136
M14	VSS_60	VSS_137
M13	VSS_61	VSS_138
M12	VSS_62	VSS_139
M6	VSS_63	VSS_140
L34	VSS_64	VSS_141
L33	VSS_65	VSS_142
L30	VSS_66	VSS_143
L29	VSS_67	VSS_144
K38	VSS_68	VSS_145
K11	VSS_69	VSS_146
K10	VSS_70	VSS_147
K9	VSS_71	VSS_148
K8	VSS_72	VSS_149
K7	VSS_73	VSS_150
K5	VSS_74	VSS_151
K4	VSS_75	VSS_152
K3	VSS_76	VSS_153
K2	VSS_77	VSS_154

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KABYLAKE-H-CPU_BGA1440

UC1L SKYLAKE_HALO		
BGA1440		
C17	VSS_154	VSS_239
C13	VSS_155	VSS_240
C9	VSS_156	VSS_241
BT32	VSS_157	VSS_242
BT26	VSS_158	VSS_243
BT24	VSS_159	VSS_244
BT21	VSS_160	VSS_245
BT18	VSS_161	VSS_246
BT14	VSS_162	VSS_247
BT12	VSS_163	VSS_248
BT9	VSS_164	VSS_249
BT5	VSS_165	VSS_250
BR36	VSS_166	VSS_251
BR34	VSS_167	VSS_252
BR29	VSS_168	VSS_253
BR26	VSS_169	VSS_254
BR24	VSS_170	VSS_255
BR21	VSS_171	VSS_256
BR18	VSS_172	VSS_257
BR14	VSS_173	VSS_258
BR12	VSS_174	VSS_259
BR7	VSS_175	VSS_260
BP34	VSS_176	VSS_261
BP33	VSS_177	VSS_262
BP29	VSS_178	VSS_263
BP26	VSS_179	VSS_264
BP24	VSS_180	VSS_265
BP21	VSS_181	VSS_266
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BP14	VSS_183	VSS_268
BP12	VSS_184	VSS_269
BP7	VSS_185	VSS_270
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BN31	VSS_187	VSS_272
BN30	VSS_188	VSS_273
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BM18	VSS_201	VSS_286
BM35	VSS_202	VSS_287
BM28	VSS_203	VSS_288
BM27	VSS_204	VSS_289
BM26	VSS_205	VSS_290
BM23	VSS_206	VSS_291
BM21	VSS_207	VSS_292
BM13	VSS_208	VSS_293
BM12	VSS_209	VSS_294
BM9	VSS_210	VSS_295
BM6	VSS_211	VSS_296
BM2	VSS_212	VSS_297
BL29	VSS_213	VSS_298
BK29	VSS_214	VSS_299
BK15	VSS_215	
BK14	VSS_216	
BJ32	VSS_217	
BJ31	VSS_218	
BJ25	VSS_219	
BJ22	VSS_220	
BH14	VSS_221	
BH12	VSS_222	
BH9	VSS_223	
BH8	VSS_224	
BH5	VSS_225	
BH4	VSS_226	
BH1	VSS_227	
BG38	VSS_228	
BG13	VSS_229	
BG12	VSS_230	
BF33	VSS_231	
BF12	VSS_232	
BE29	VSS_233	
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BD9	VSS_235	
BC34	VSS_236	
BC12	VSS_237	
BB12	VSS_238	

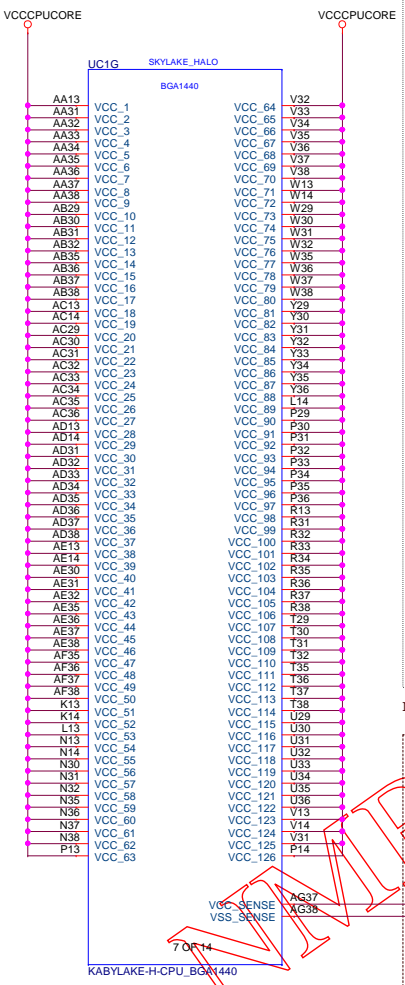
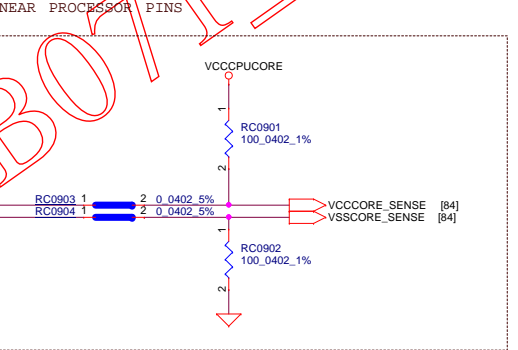
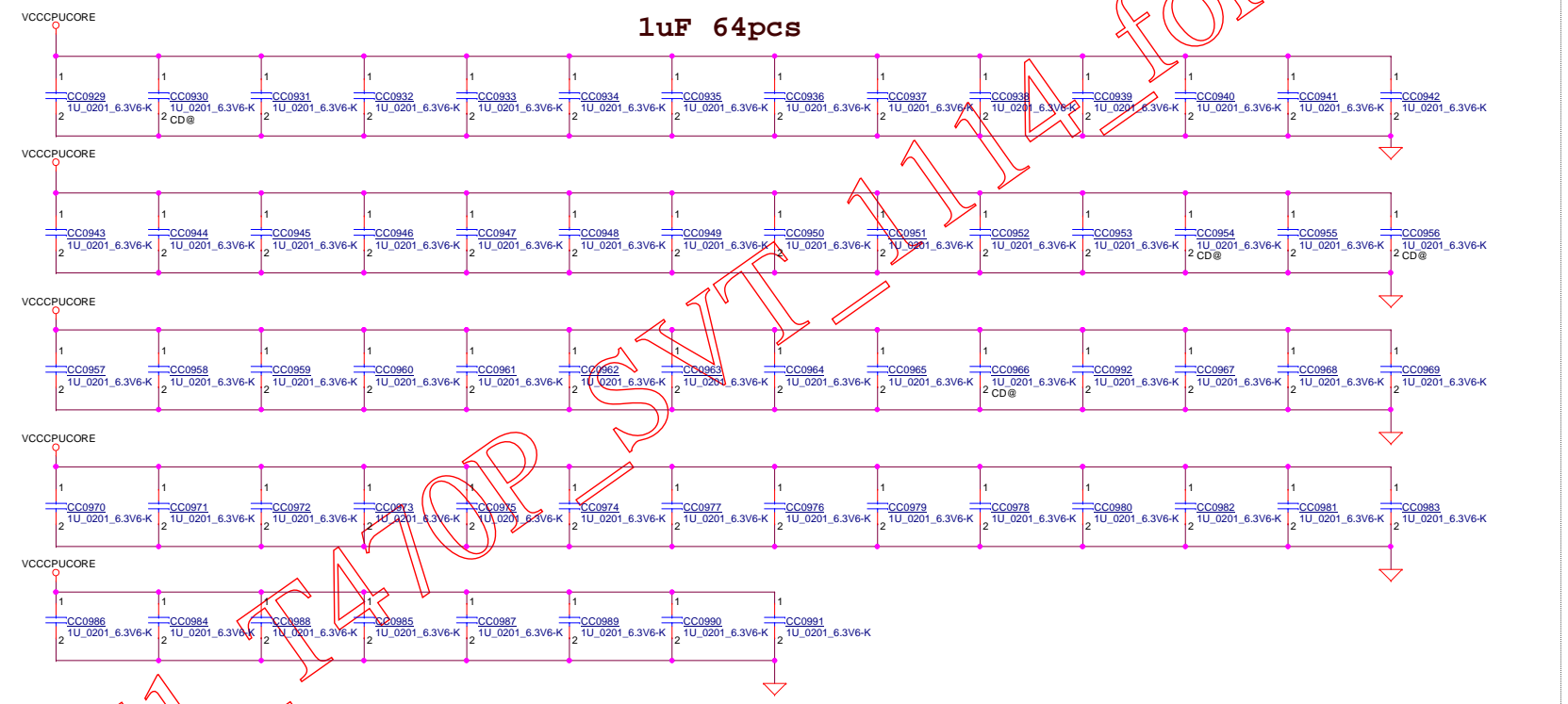
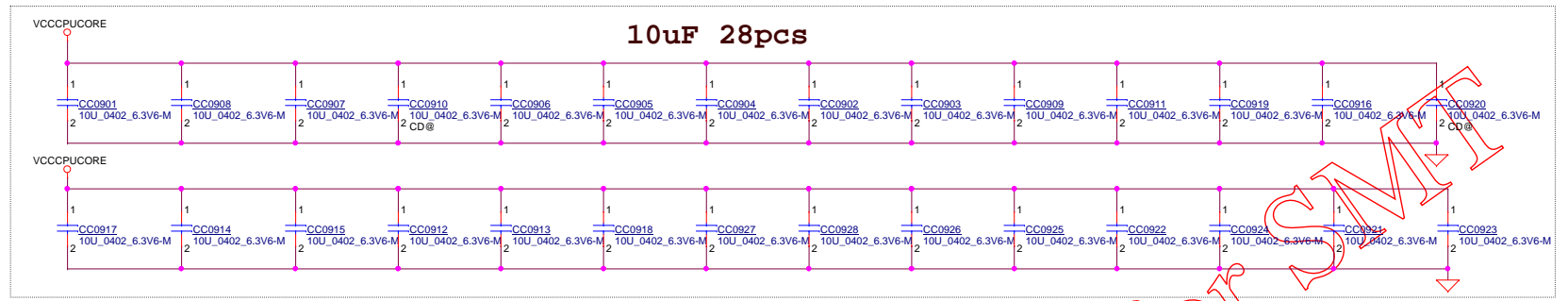
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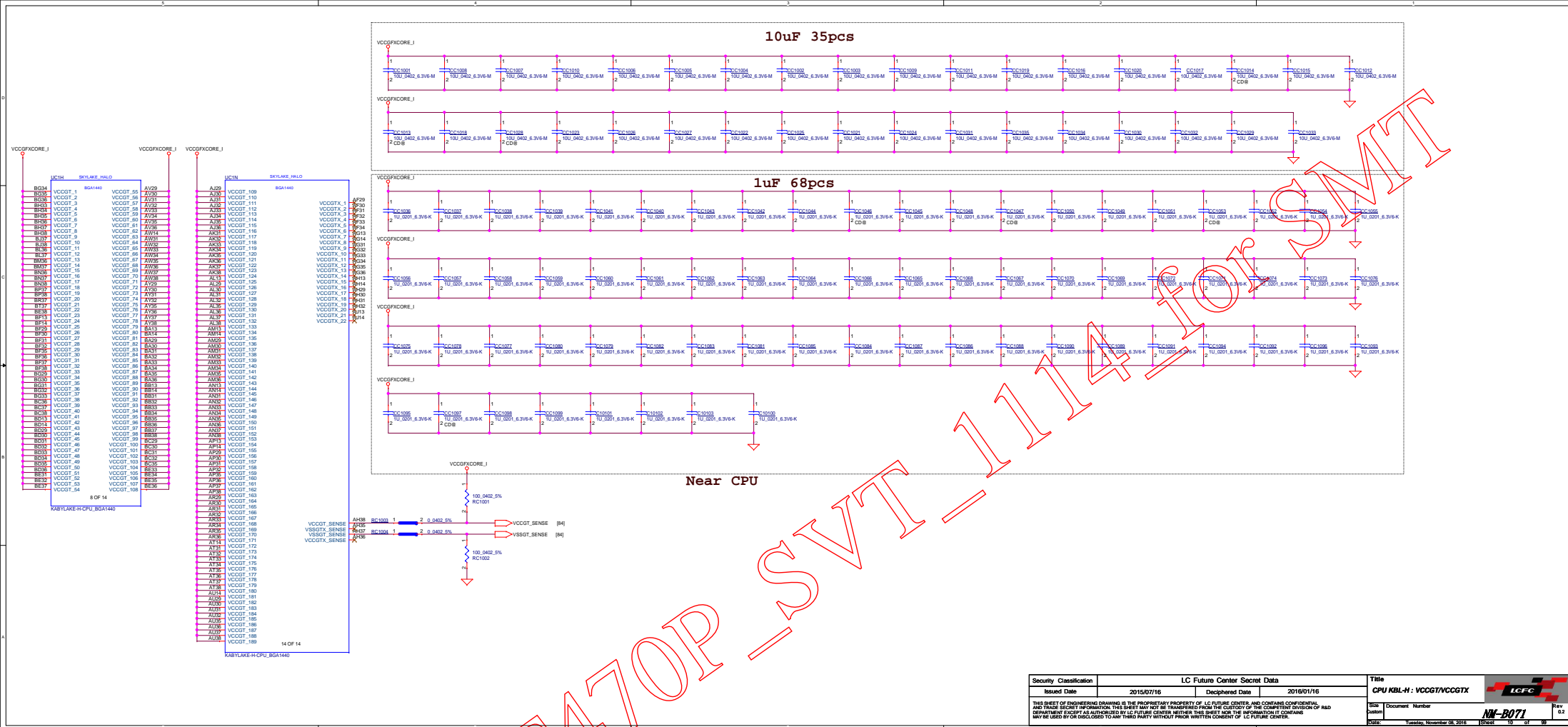
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BA37	VSS_305	VSS_383
C11	VSS_306	VSS_384
C8	VSS_307	VSS_385
BA11	VSS_308	VSS_386
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BA9	VSS_310	VSS_388
BA8	VSS_311	VSS_389
BA7	VSS_312	VSS_390
BA6	VSS_313	VSS_391
BA5	VSS_314	VSS_392
AY34	VSS_315	VSS_393
AY33	VSS_316	VSS_394
AY12	VSS_317	VSS_395
AW30	VSS_318	VSS_396
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AV37	VSS_326	VSS_404
AU34	VSS_327	VSS_405
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AU12	VSS_329	VSS_407
AU11	VSS_330	VSS_408
AU10	VSS_331	VSS_409
AU9	VSS_332	VSS_410
AU8	VSS_333	VSS_411
AU7	VSS_334	VSS_412
AU6	VSS_335	VSS_413
AT30	VSS_336	VSS_414
AT29	VSS_337	VSS_415
AT6	VSS_338	VSS_416
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AP10	VSS_352	VSS_430
AP9	VSS_353	VSS_431
AP8	VSS_354	VSS_432
AN30	VSS_355	VSS_433
AN29	VSS_356	VSS_434
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AM4	VSS_364	VSS_442
AM3	VSS_365	VSS_443
AM2	VSS_366	VSS_444
AM1	VSS_367	VSS_445
AL34	VSS_368	VSS_446
AL33	VSS_369	
AL12	VSS_370	
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AL9	VSS_372	
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	VSS_376	
	VSS_377	

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KABYLAKE-H-CPU_BGA1440

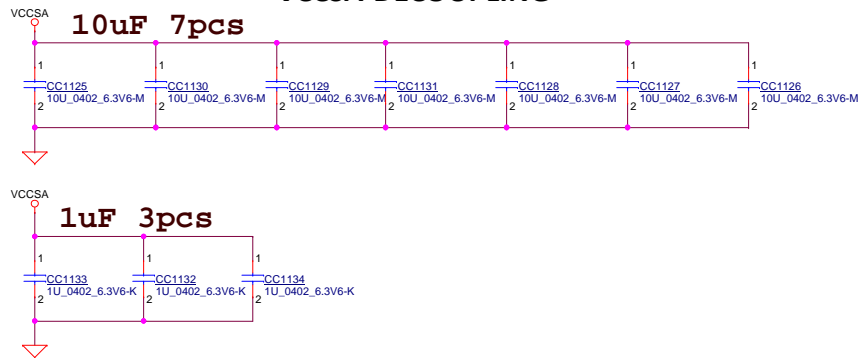
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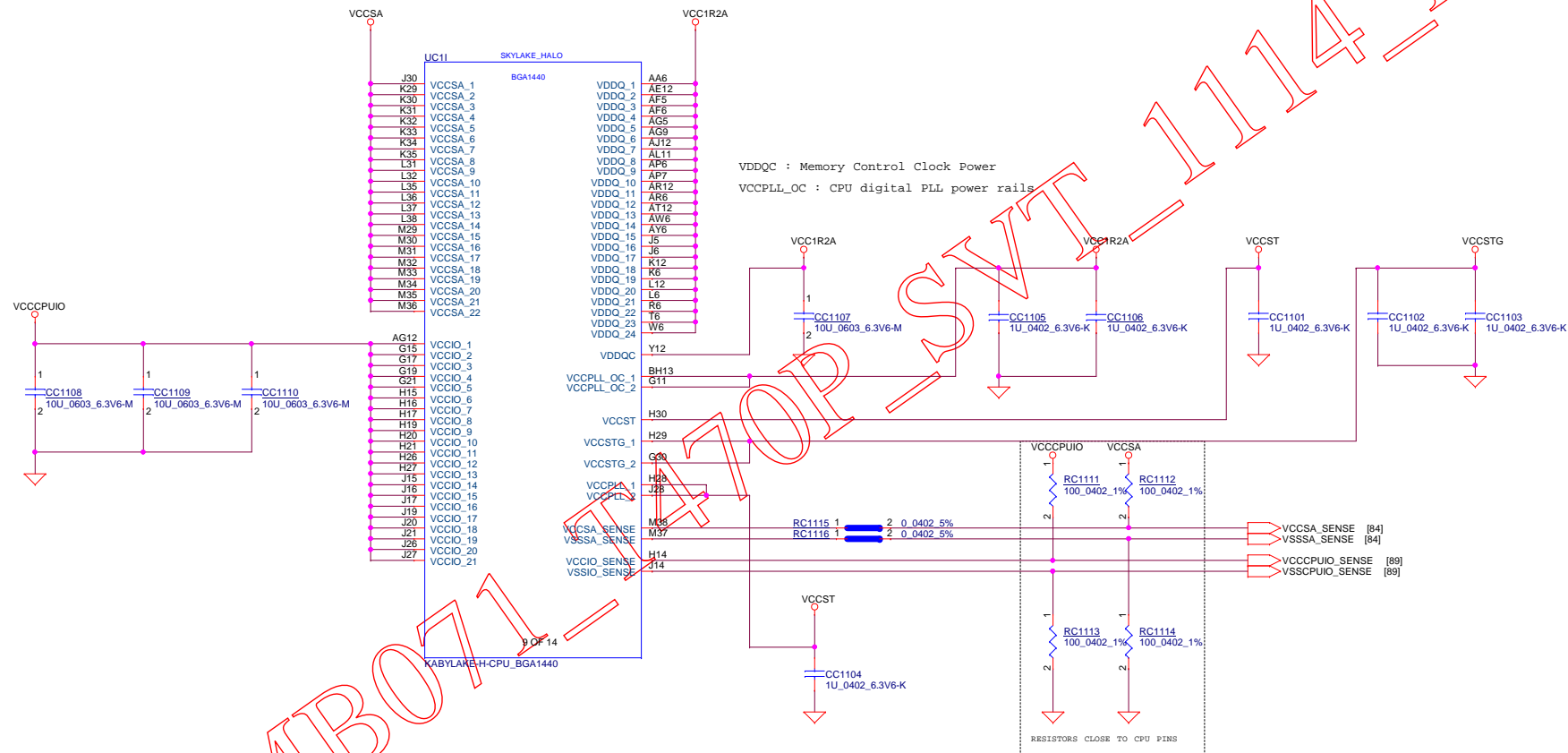
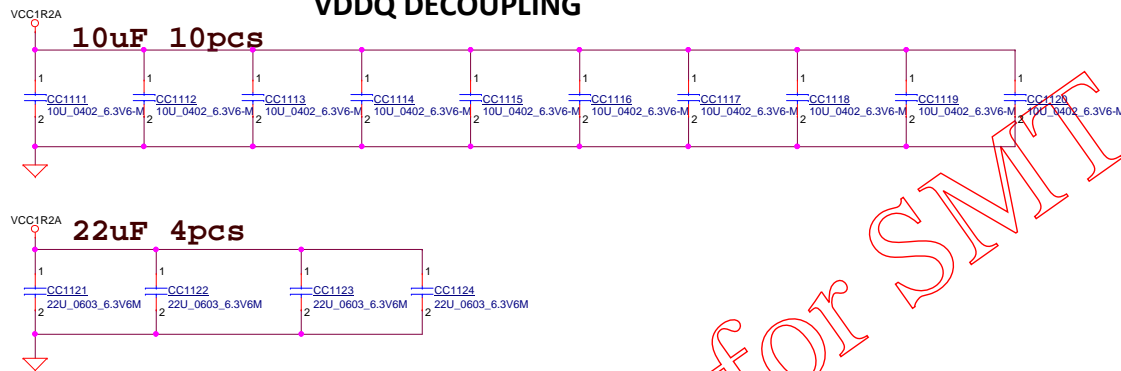
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VDDQ DECOUPLING



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Security Classification		LC Future Center Secret Data		Title		
Issued Date	2015/07/16	Deciphered Date	2016/01/16	CPU KBL-H : VCCSA/VCCIO/VDDQ		
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Size	Document	Number		Rev		
Custom				0.2		
Date:	Tuesday, November 08, 2016		Sheet	11	of 99	

NMB071-T470-SVT-1114-for-SMT

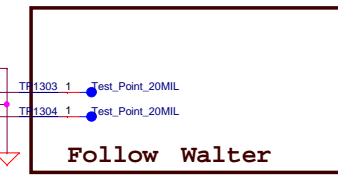
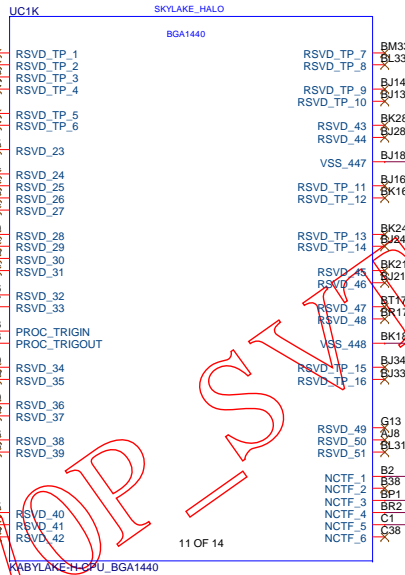
OPC RCOM Support 4+4e
If not use can't conector

UC1J SKYLAKE_HALO	
BGA1440	
BJ17	VCCOPC_1
BJ18	VCCOPC_2
BJ20	VCCOPC_3
BK17	VCCOPC_4
BK18	VCCOPC_5
BL18	VCCOPC_6
BL17	VCCOPC_7
BL18	VCCOPC_8
BL19	VCCOPC_9
BL20	VCCOPC_10
BL21	VCCOPC_11
BL22	VCCOPC_12
BM17	VCCOPC_13
BN17	VCCOPC_14
BJ23	RSVD_1
BJ26	RSVD_2
BK23	RSVD_3
BK26	RSVD_4
BL23	RSVD_5
BL24	RSVD_6
BL25	RSVD_7
BL26	RSVD_8
BL27	RSVD_9
BL28	RSVD_10
BL29	RSVD_11
BM24	RSVD_12
	RSVD_13
BL15	VCCOPC_SENSE
BM16	VSSOPC_SENSE
BL22	RSVD_14
BM22	RSVD_15
BP15	VCCEOPIO_1
BR15	VCCEOPIO_2
BT15	VCCEOPIO_3
BP16	RSVD_16
BR16	RSVD_17
BT16	RSVD_18
BN15	VCCEOPIO_SENSE
BM15	VSSEOPIO_SENSE
BP17	RSVD_19
BN16	RSVD_20
BM14	VCC_OPC_1P8_1
BL14	VCC_OPC_1P8_2
BJ15	RSVD_21
BJ16	RSVD_22
AT13	ZVM#
AW13	MSM#
AU13	ZVM2#
AY13	MSM2#
BT29	OPC_RCOMP
BR29	OPCE_RCOMP
BP29	OPCE_RCOMP2
10 OF 14	
KABYLAKE-H-CPU_BGA1440	

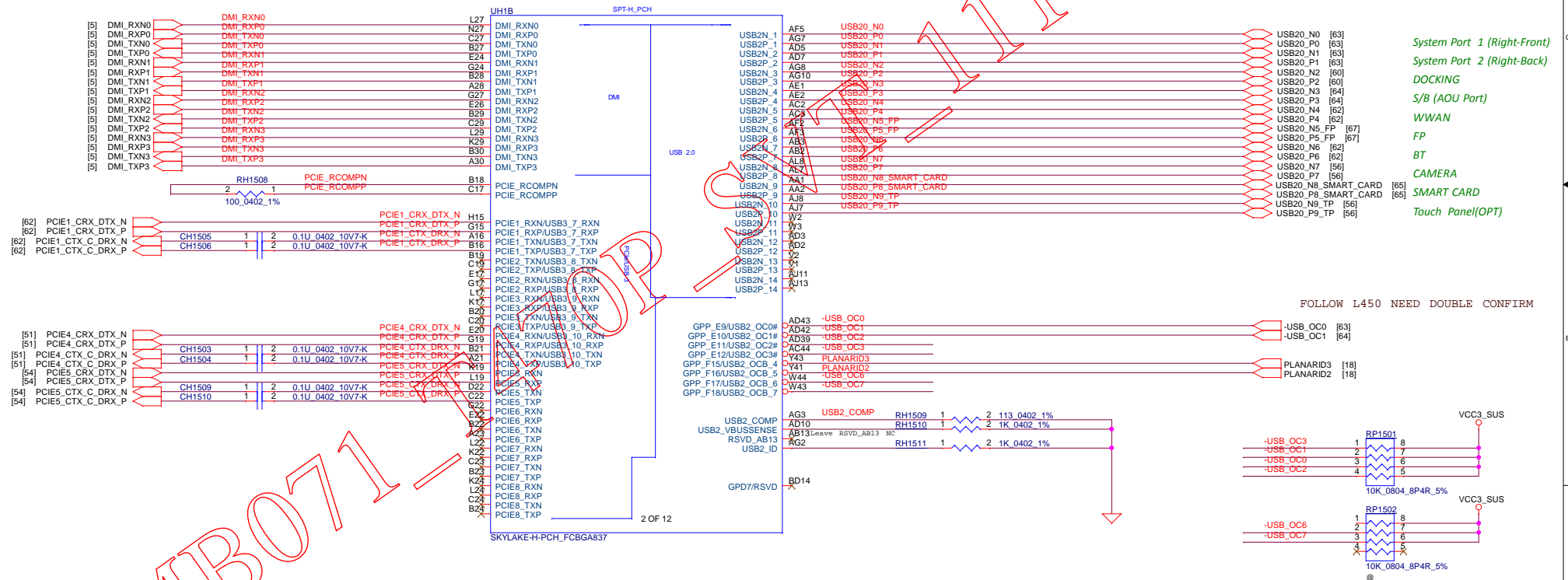
Follow Intel Spec document Rev. 0.75.
A36,A37 change to VSS

[22] PCH_2_CPU_TRIGGER
[22] CPU_2_PCH_TRIGGER

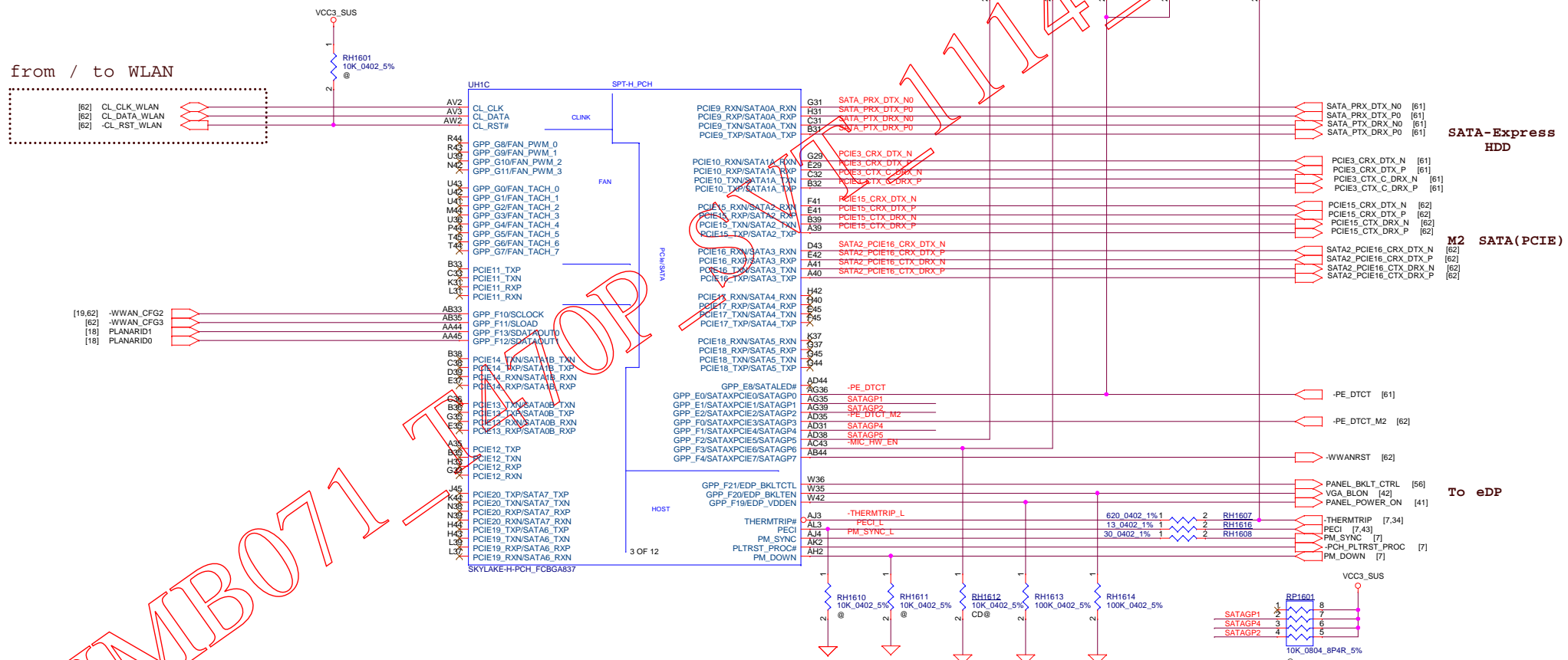
RC1301 2 1 30.0402 1% CPU_2_PCH_TRIGGER R



USB2.0	Port Assignment	OC#
USB2 #1	Non-AOU port 1	OC0#
USB2 #2	Non-AOU port 2	OC0#
USB2 #3	Docking USB2	OC1#
USB2 #4	AOU port	
USB2 #5	WWAN	
USB2 #6	Finger printer	
USB2 #7	BT	
USB2 #8	Camera	
USB2 #9	Smart card reader	
USB2 #10	Touch panel	
USB2 #11		
USB2 #12		



Port#	Flexible I/O	Configuration	Port Assignment
22	PCIe #16 SATA #3	SATA #3 /PCIe #13	M.2 SATA SSD / Optane
21	PCIe #15 SATA #2	PCIe #14(Reversal)	Optane
20	PCIe #14 SATA #1		
19	PCIe #13 SATA #0 GbE		
18	PCIe #12 GbE		
17	PCIe #11		
16	PCIe #10 SATA #1	PCIe #10	SATA-Express
15	PCIe #9 SATA #0 GbE	SATA #0/PCIe #9	SATA-Express
14	PCIe #8		
13	PCIe #7		
12	PCIe #6		
11	PCIe #5 GbE	PCIe #5	Card reader
10	USB3 #10 PCIe #4 GbE	PCIe #4	GbE PHY
09	USB3 #9		
08	USB3 #8		
07	USB3 #7	PCIe #1	WLAN
06	USB3 #6		
05	USB3 #5		
04	USB3 #4	USB3 #4	Docking USB3
03	USB3 #3	USB3 #3	USB AOU port
02	USB3 #2	USB3 #2	USB non AOU port
01	USB3 #1	USB3 #1	USB non AOU port



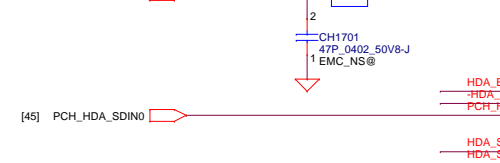
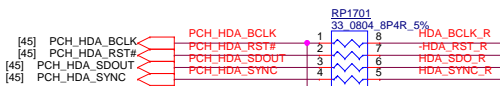
- Notes:**
- The SRCCLKREQ#[15:0] signals can be configured to map to any of the PCH-H PCI Express* Root Ports
 - SRCCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements
 - SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs
 - SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/07/16	Deciphered Date	2016/01/16	PCHSKL-H : SATA/PCIe	
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Size	Document	Number		Rev	
Custom				0.2	
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TABLE : Functional Strap

HDA_SDO	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

HDA_SDO is used to update the Descriptor and/or the ME regions of the SPI after MFG Done bit is set.



20140730: As of now, we cannot get information about these pins from SKL-H RVP and other documents. We need to confirm about them later.

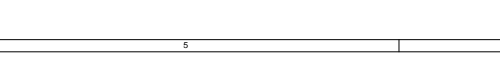
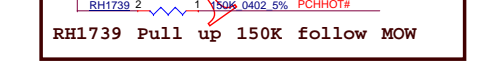
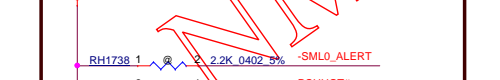
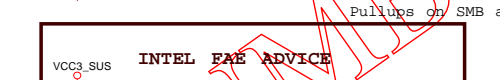
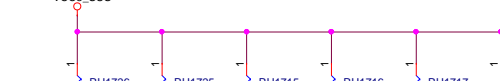
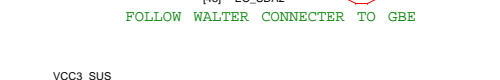
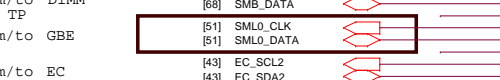
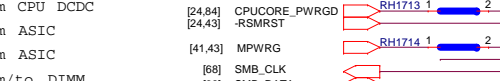
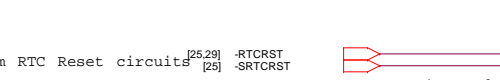
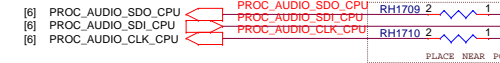


TABLE : Functional Strap

GPP_C5/SML0ALERT#(LPC or SPI)	
HIGH	eSPI is selected
LOW	LPC is selected(Default)

TABLE : Functional Strap

GPP_C5/SML0ALERT#(TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS(Default)

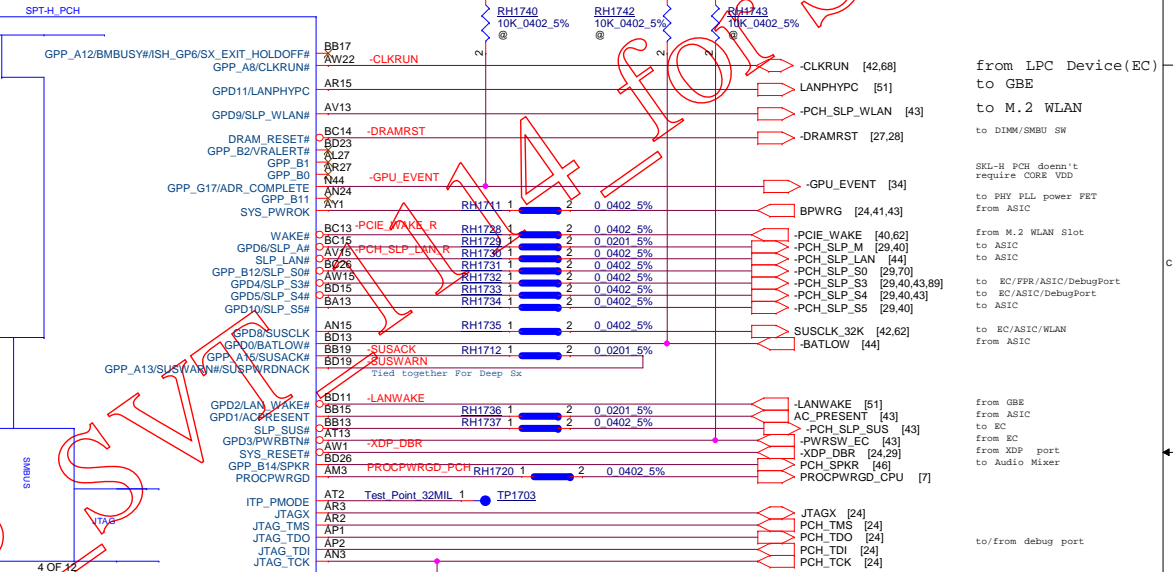
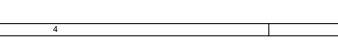
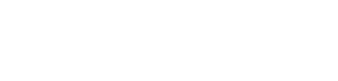
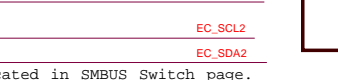
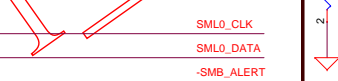
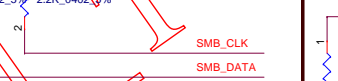
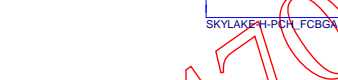
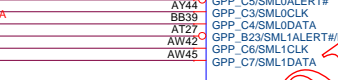
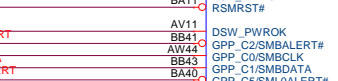
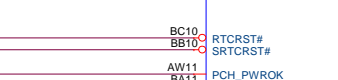
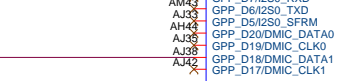
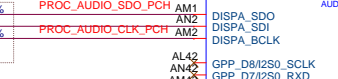
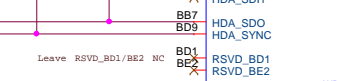
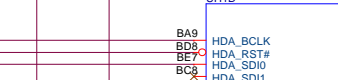
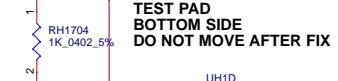
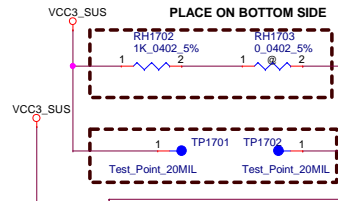
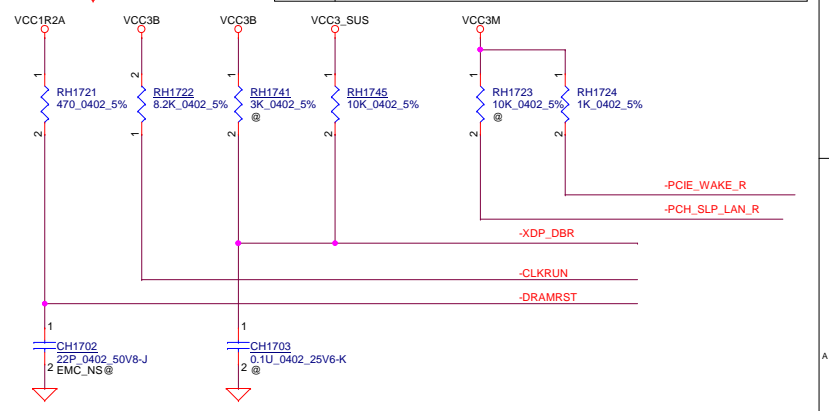
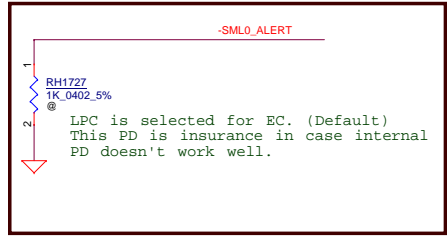


TABLE : Functional Strap

GPP_B14/SPKR(Top Swap Override)	
HIGH	Enable "TOP Swap" Mode
LOW	Disable "TOP Swap" Mode (Default by Internal PD)



important



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Issued Date	2015/07/16	Deciphered Date	2016/01/16	PCH SKL-H : AUDIO/SMBUS/JTAG	
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				Custom	NM-B071
				Date	Tuesday, November 01, 2016
				Sheet	17 of 99

to be confirm on SDV

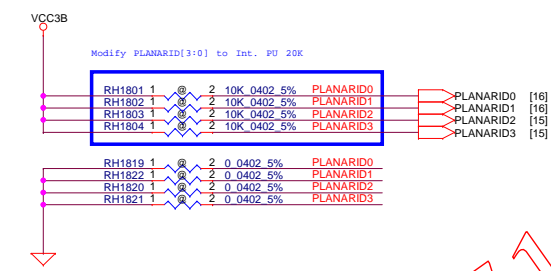
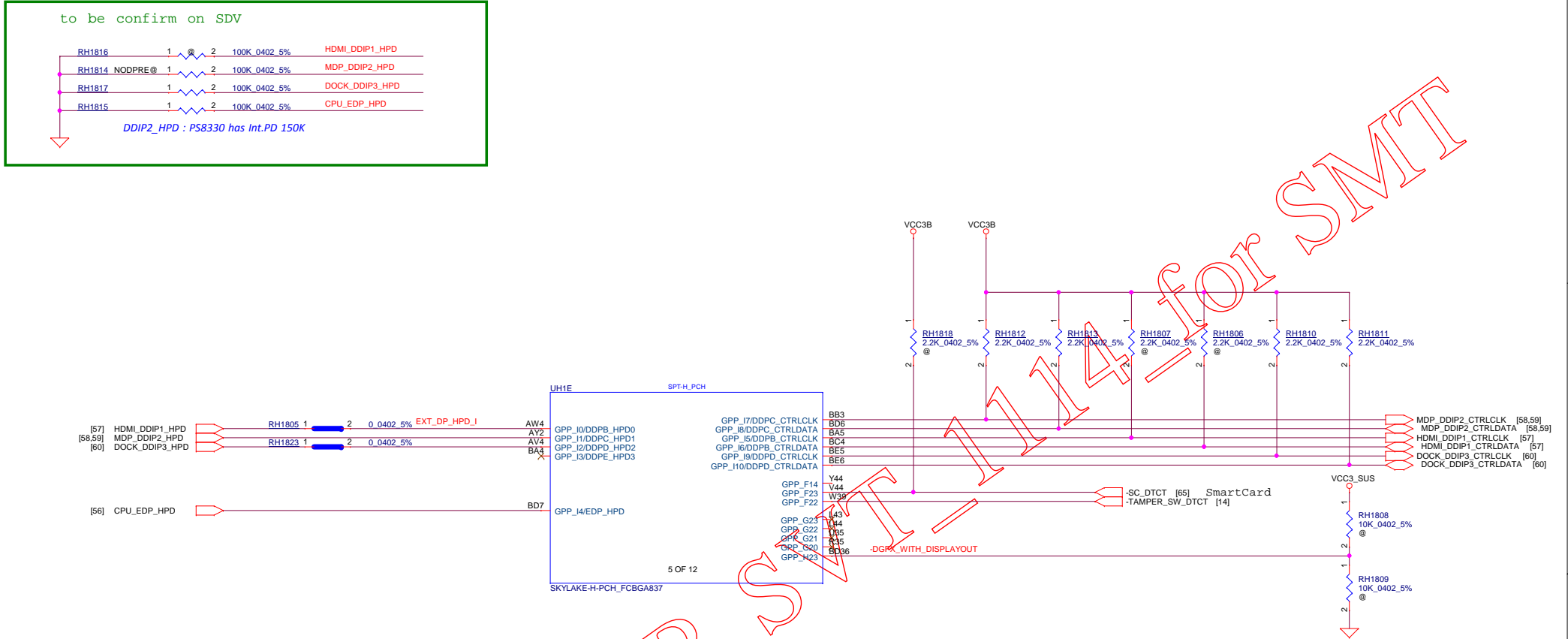
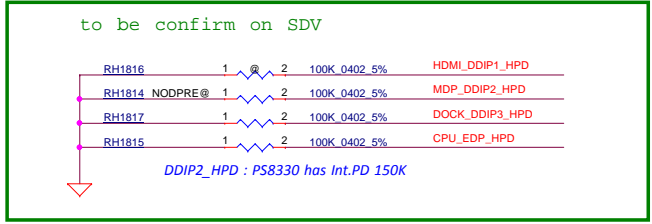
RH1816 1 2 100K 0402 5% HDMI_DDIP1_HPD

RH1814 NODPRE@ 1 2 100K 0402 5% MDP_DDIP2_HPD

RH1817 1 2 100K 0402 5% DOCK_DDIP3_HPD

RH1815 1 2 100K 0402 5% CPU_EDP_HPD

DDIP2_HPD : PS8330 has Int.PD 150K

[illegible][illegible][illegible]

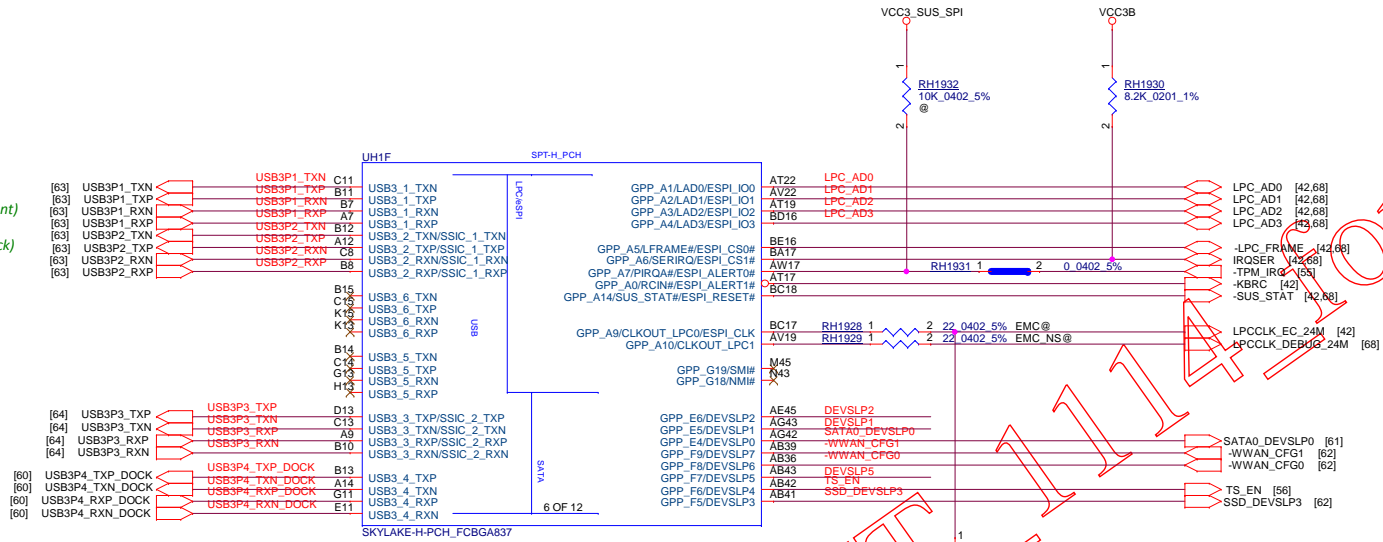
NMB071-T470P-SVT-14 for SMT

System Port 1 (Right-Front)

System Port 2 (Right-Back)

Small Board

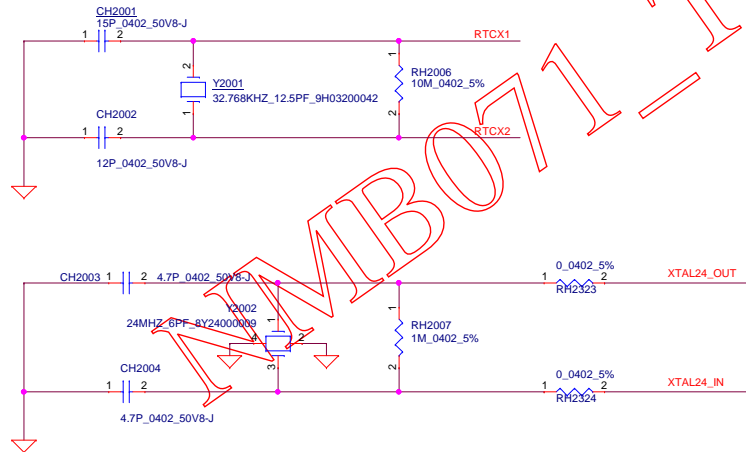
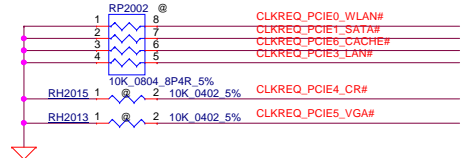
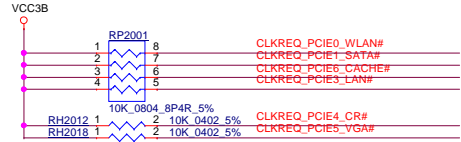
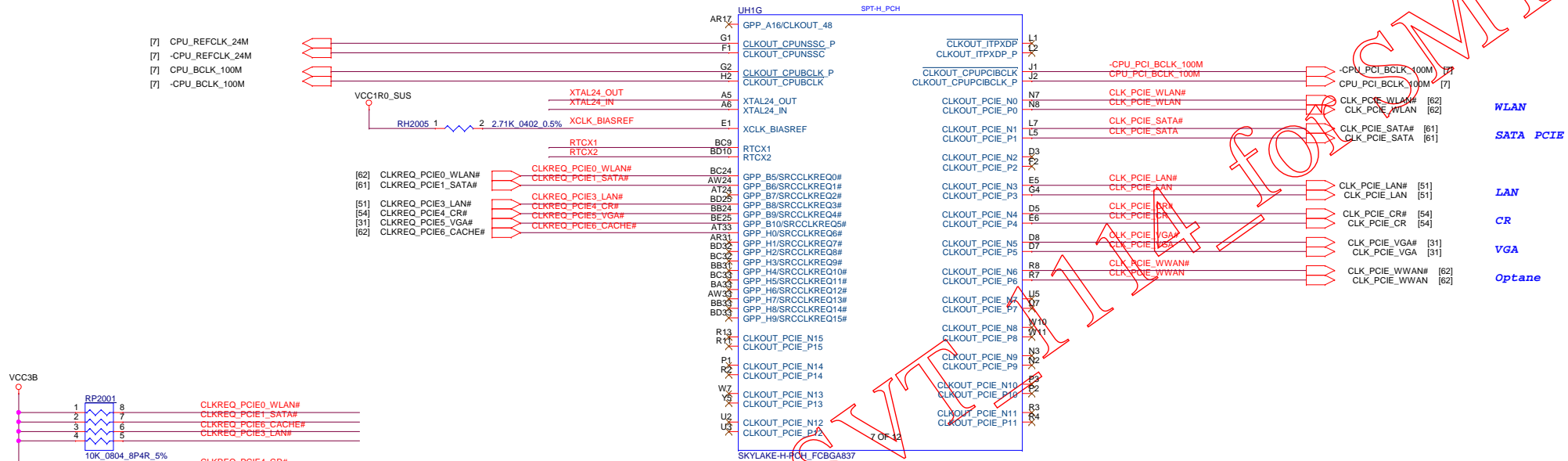
DOCKING



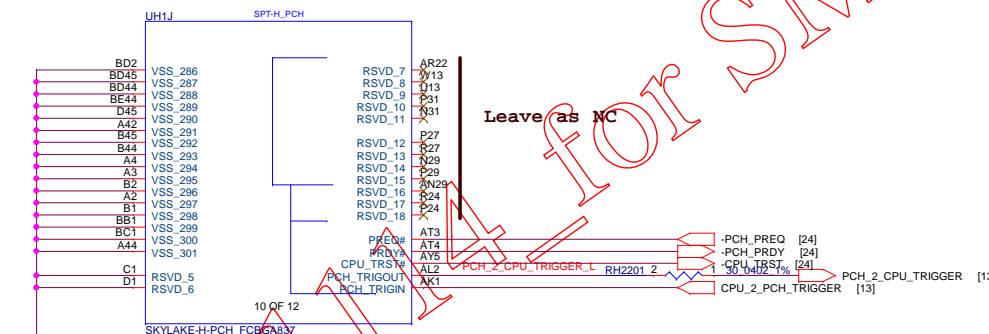
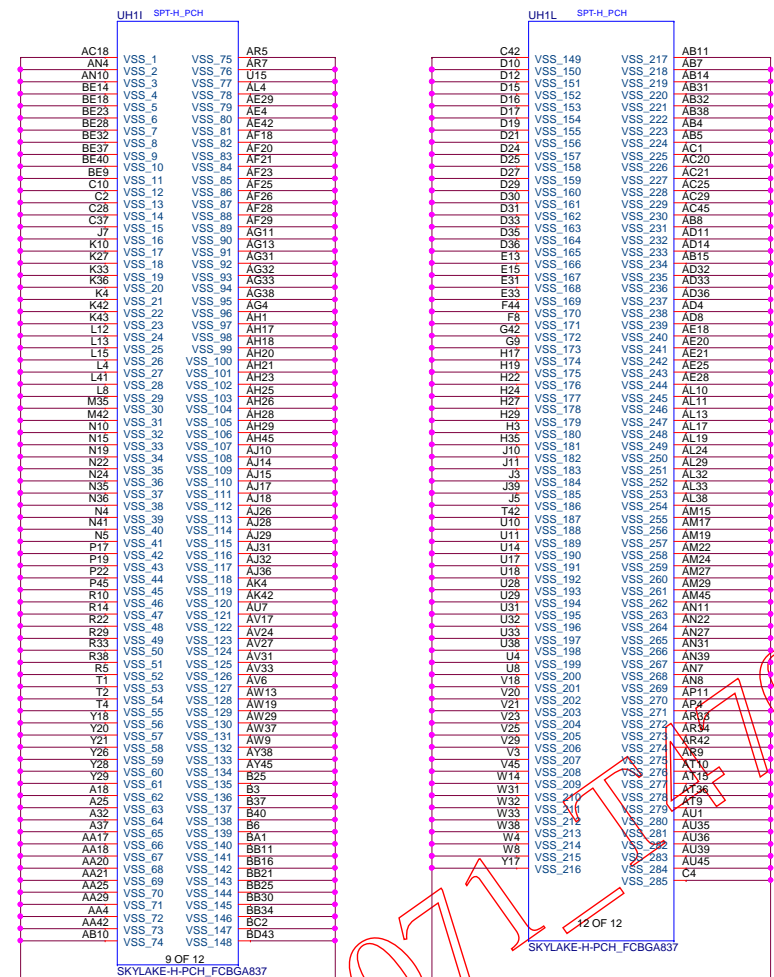
Security Classification		LC Future Center Secret Data	
Issued Date	2015/07/16	Deciphered Date	2016/01/16
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Title		LCFC	
PCH SKL-H : USB3/LPC			
Size	Document Number	Rev	
Custom	NM-B071	0.2	
Date:	Tuesday, November 01, 2016	Sheet	19 of 99

- [7] CPU_REFCLK_24M
- [7] -CPU_REFCLK_24M
- [7] CPU_BCLK_100M
- [7] -CPU_BCLK_100M



PCIE Clock Assignment	Clock Request
Clock 0 : WLAN	CLKREQ0#
Clock 1 : SATA-Express	CLKREQ1#
Clock 3 : Giga LAN	CLKREQ3#
Clock 4 : CARD READER	CLKREQ4#
Clock 5 : GPU N16S-GTR	CLKREQ5#
Clock 6 : Optane	CLKREQ6#



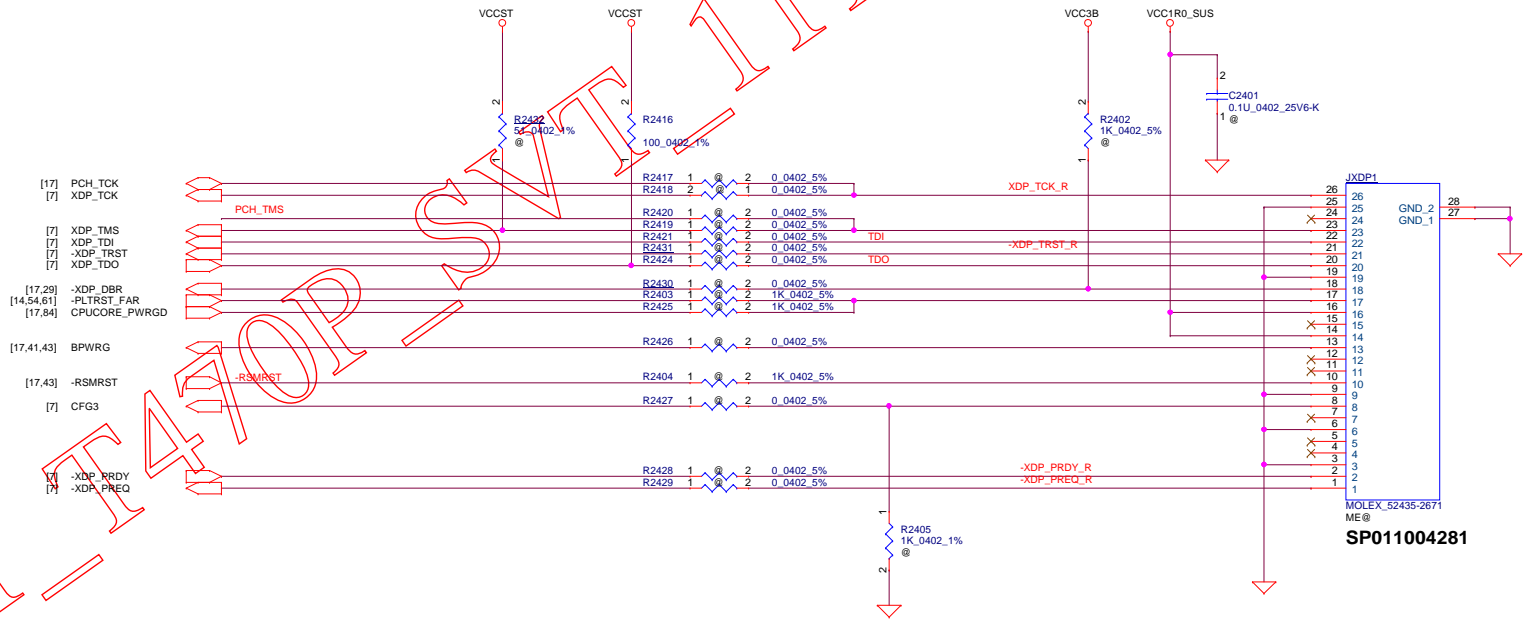
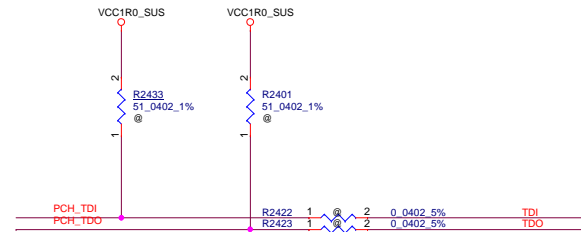
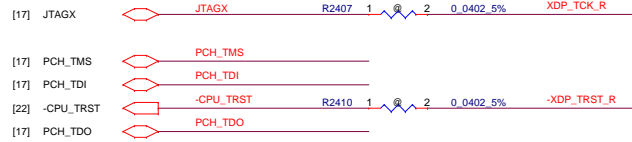


TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

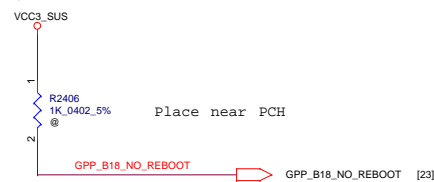
	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM


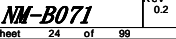
LOGIC

TABLE : Functional Strap

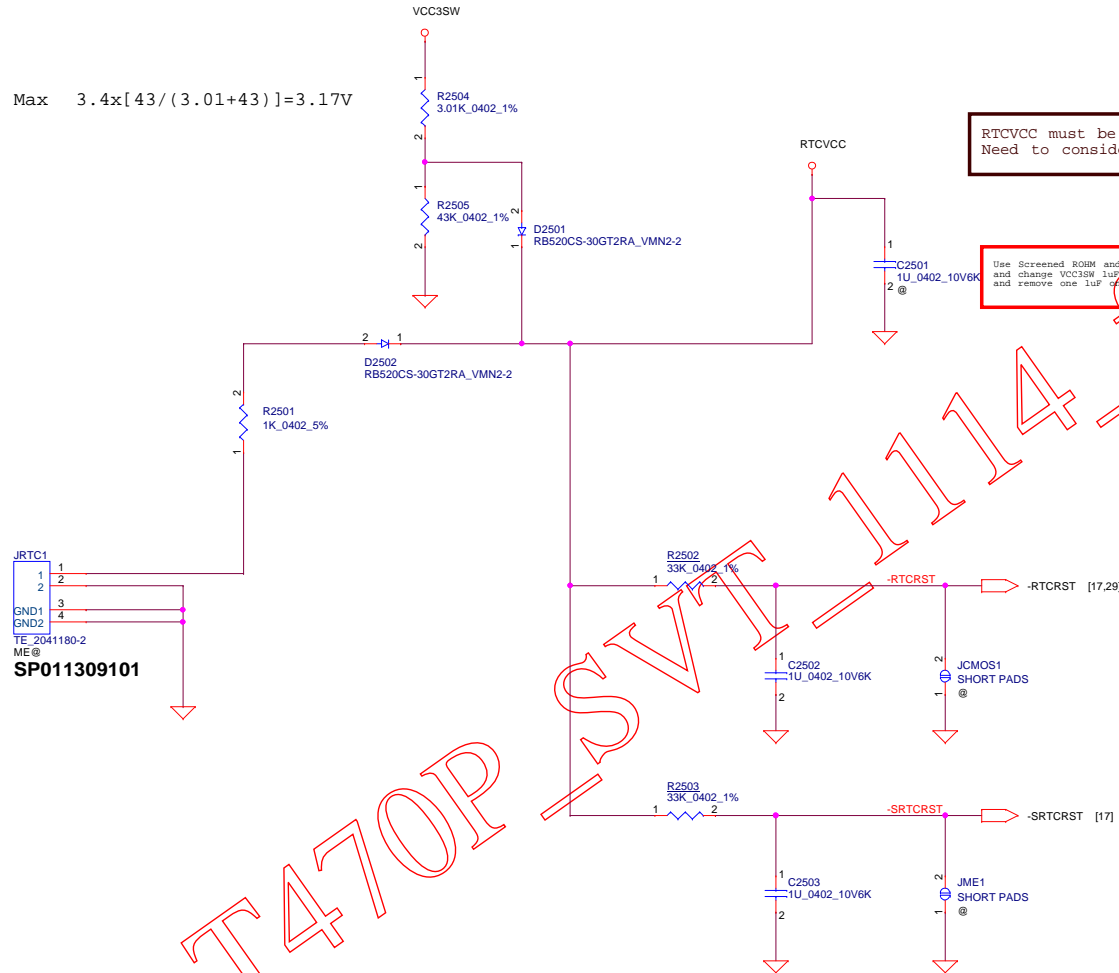
GPP_B18/GSPI0_MOSI (No Reboot)	R2406
HIGH Enable "No Reboot" Mode	ASM
LOW Disable "No Reboot" Mode (Default)	NO ASM

LOGIC



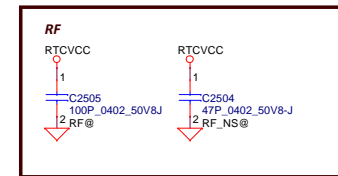
Security Classification	LC Future Center Secret Data			Title	
Issued Date	2015/07/16	Deciphered Date	2016/01/16	XDP CONNECTOR	
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$$\text{Max } 3.4 \times [43 / (3.01 + 43)] = 3.17\text{V}$$



RTCVCC must be less than 3.2V from GND. Need to consider voltage divider etc.

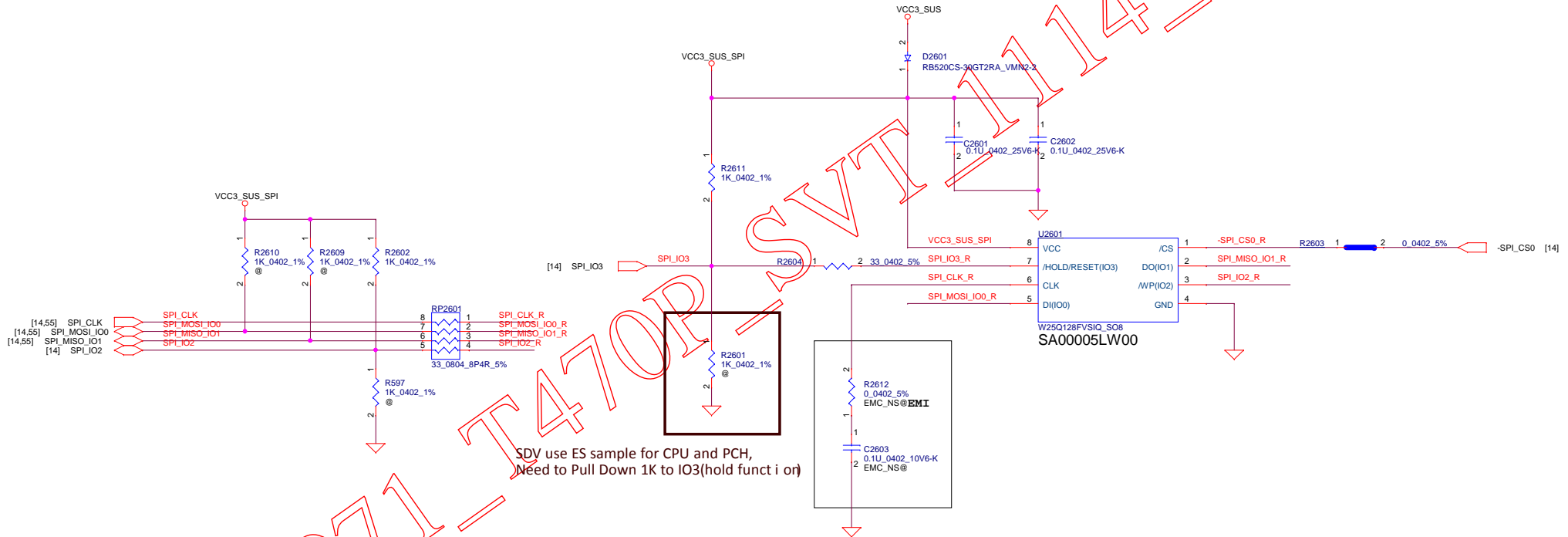
Use Screened ROHM and Toshiba, and change VCC3SW 1uF to 2.2uF and remove one 1uF of RTCVCC



U2601 SPI ROM

vPRO model(16MB)

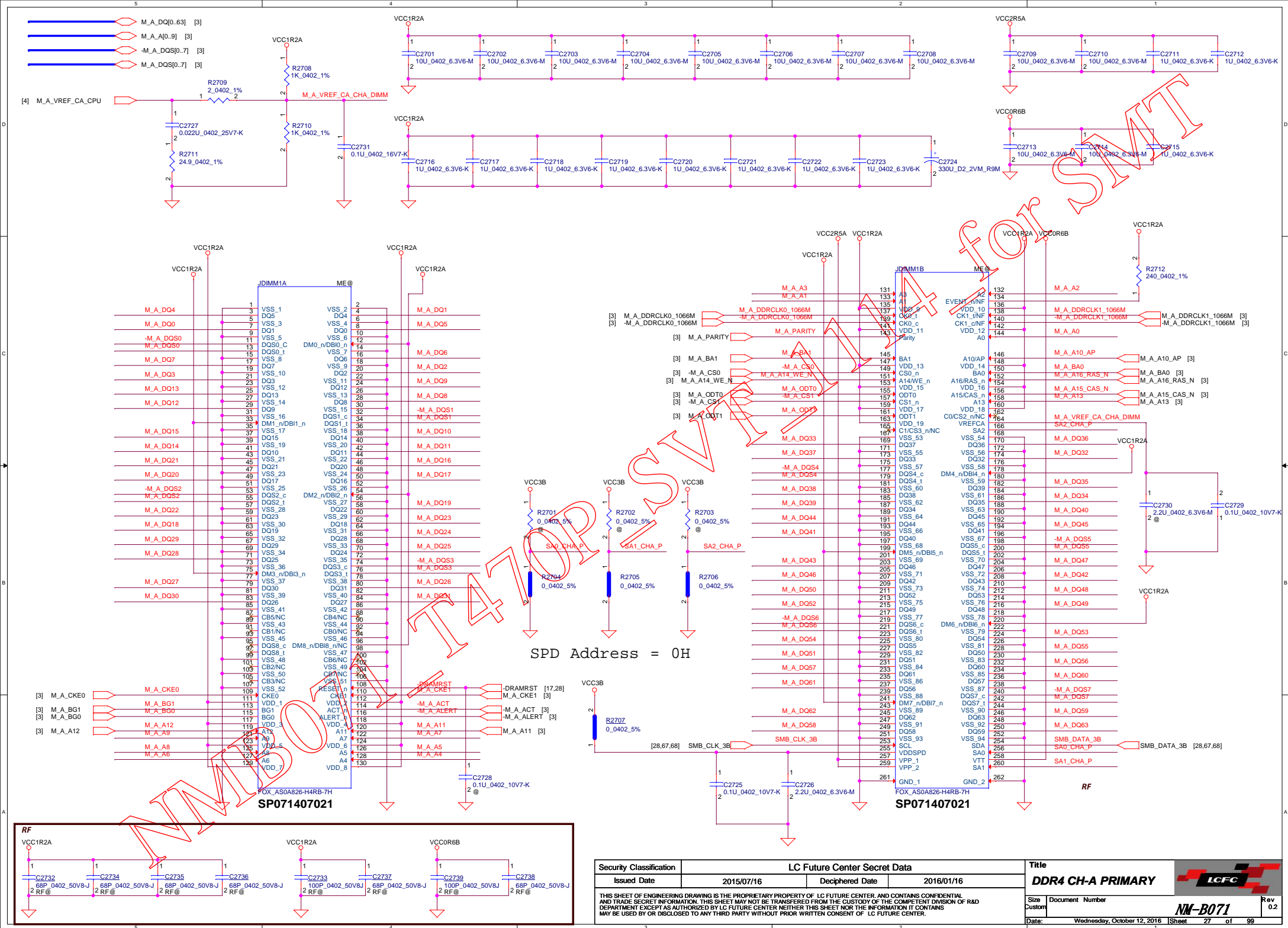
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MACRONIX MX25L12873FM2I-10G
MICRON N25Q128A13ESEC0F

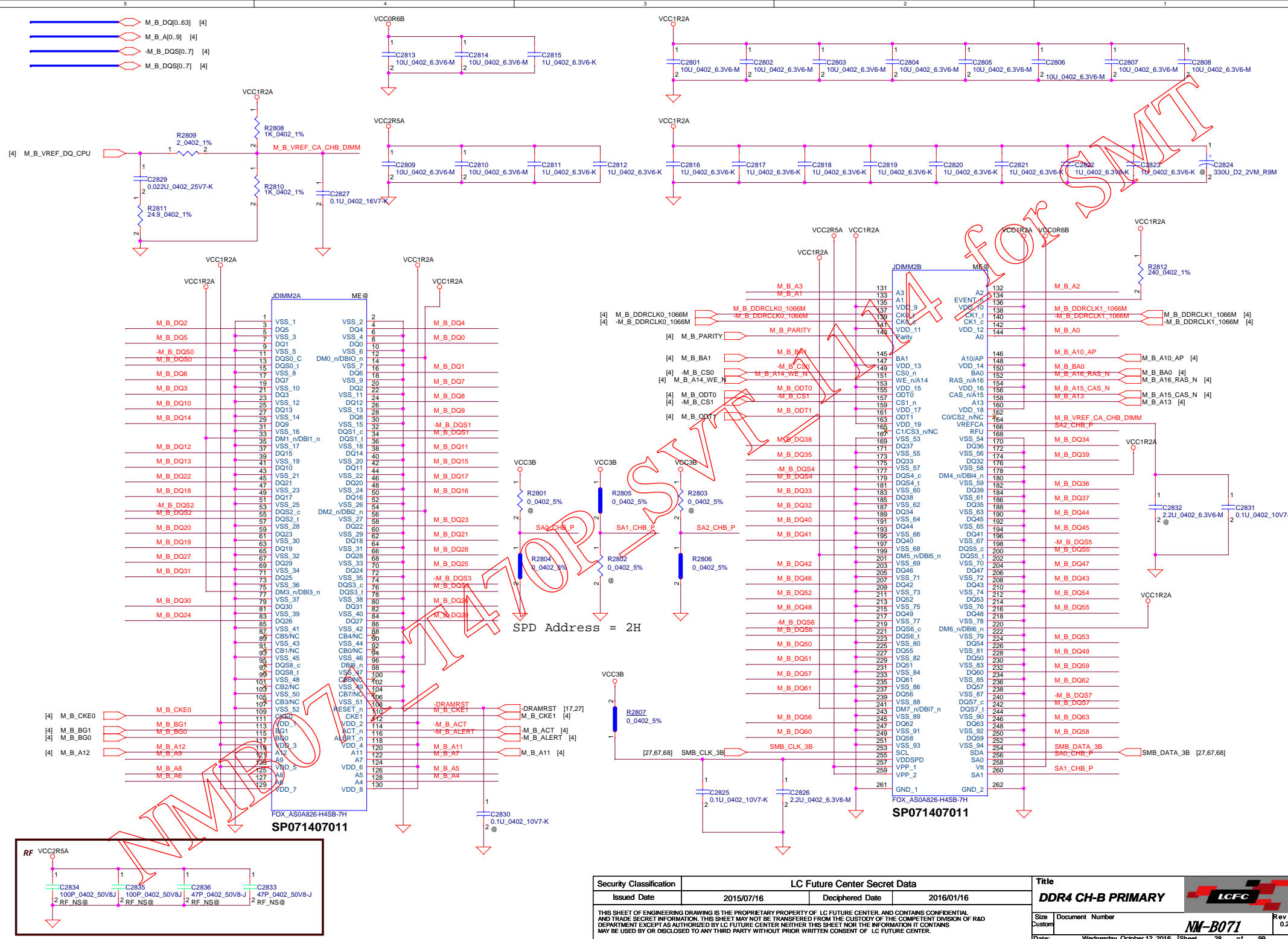



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				Date:	Wednesday, November 08, 2016



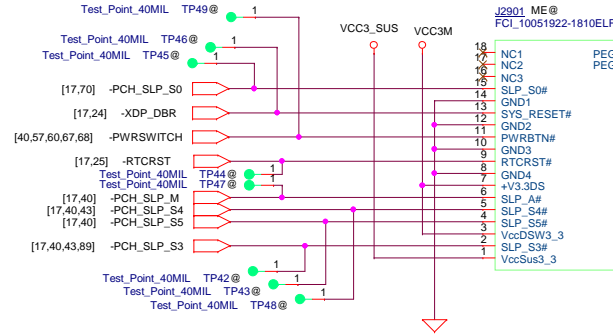
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				Custom	NM-B071
				Date:	Wednesday, October 12, 2016
				Sheet	28 of 99
				Rev	0.2

APS/PETS interface




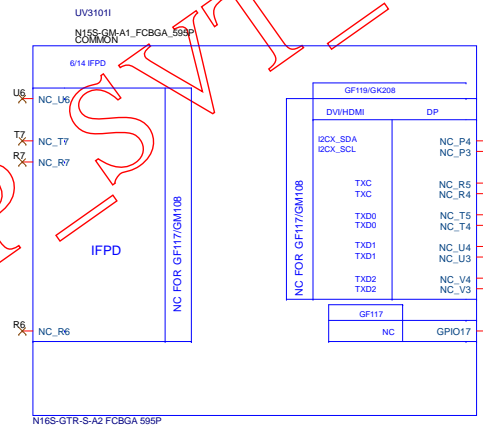
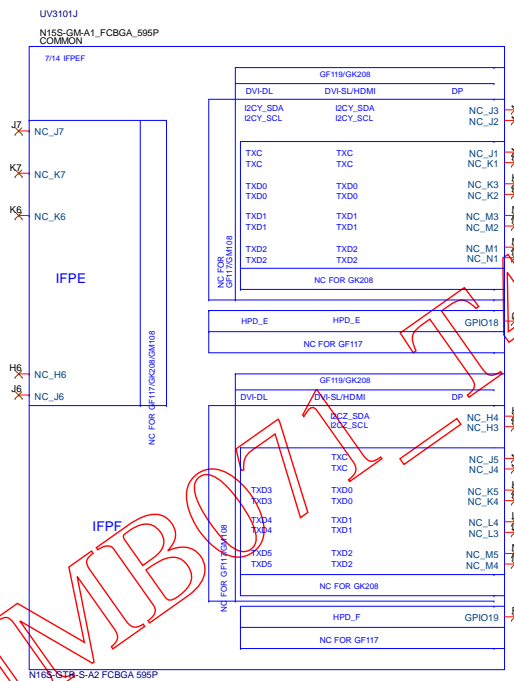
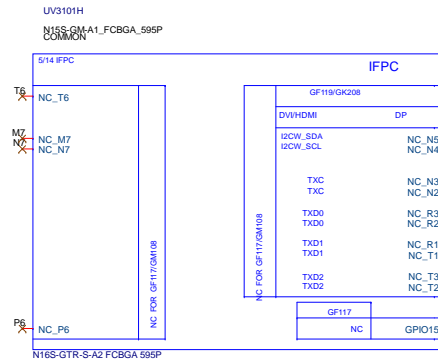
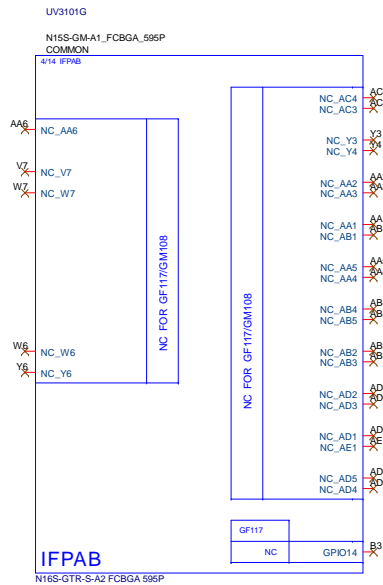
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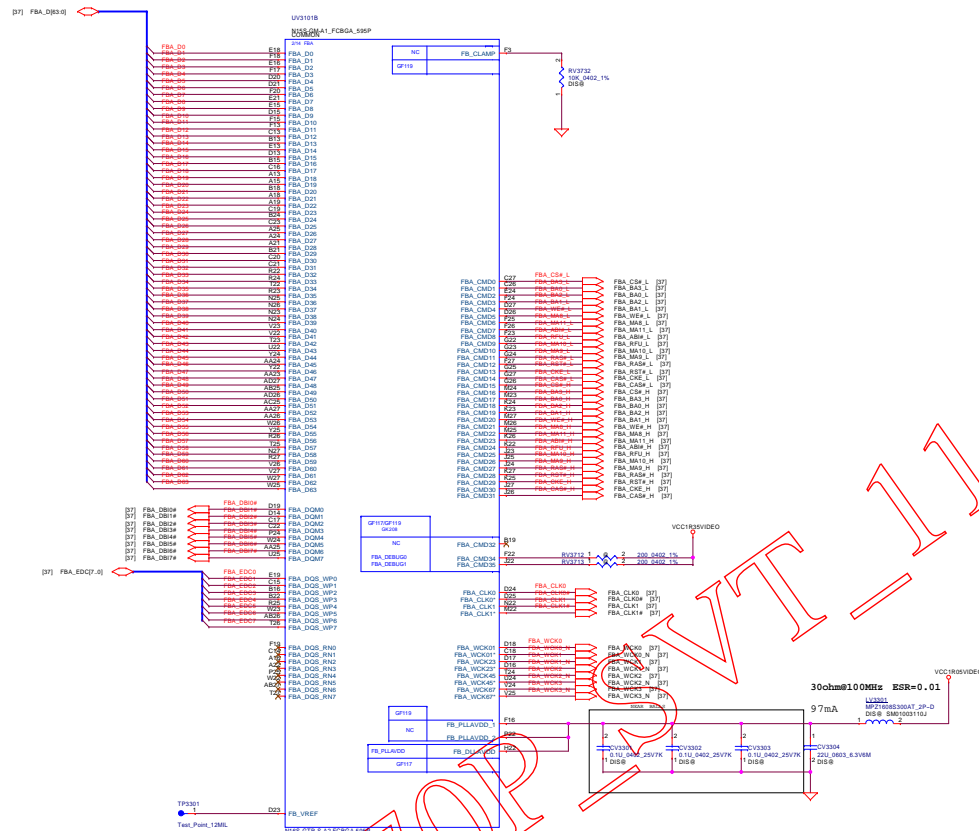
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Date:	Wednesday, October 12, 2016		Sheet	29	of	99

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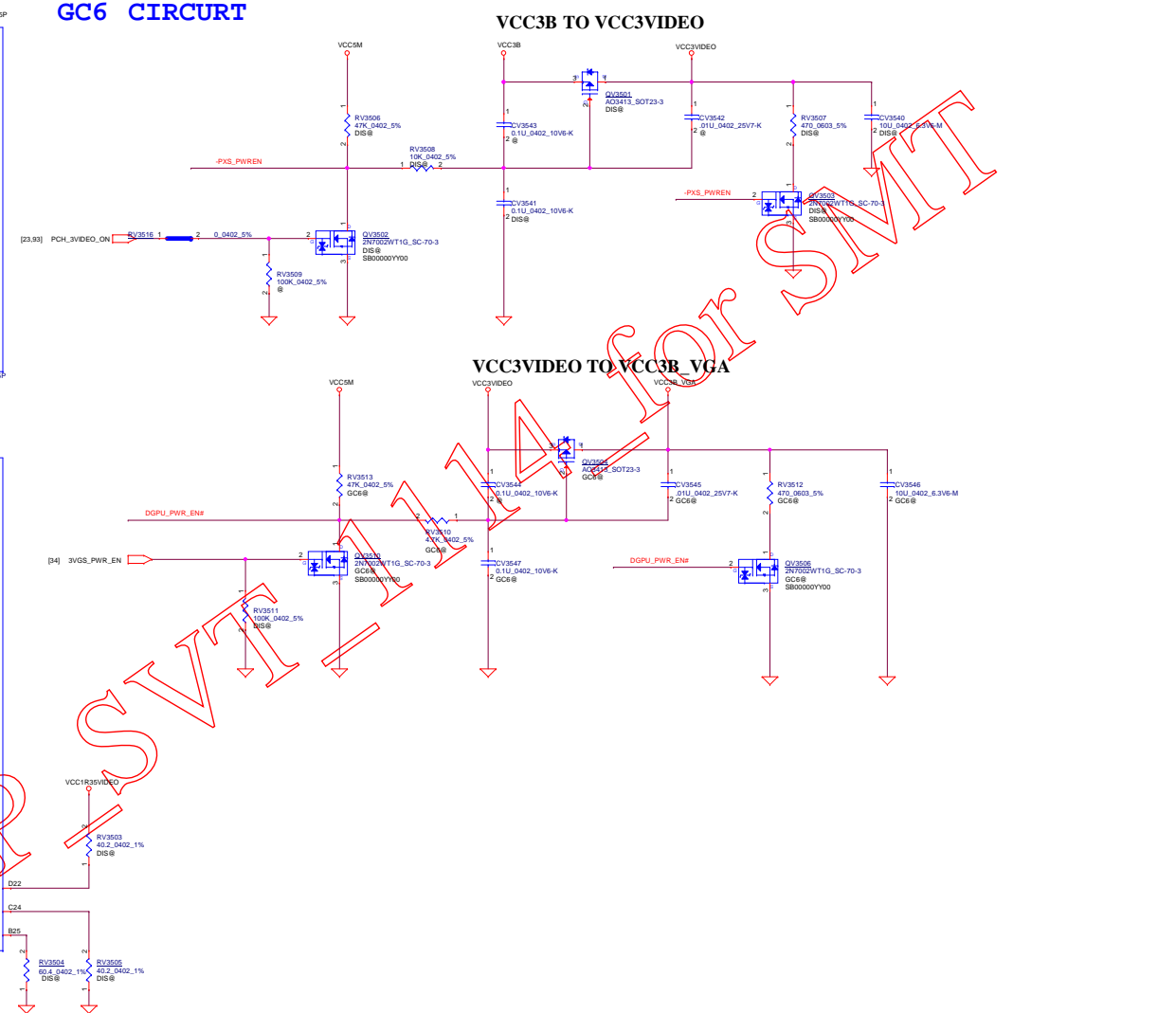
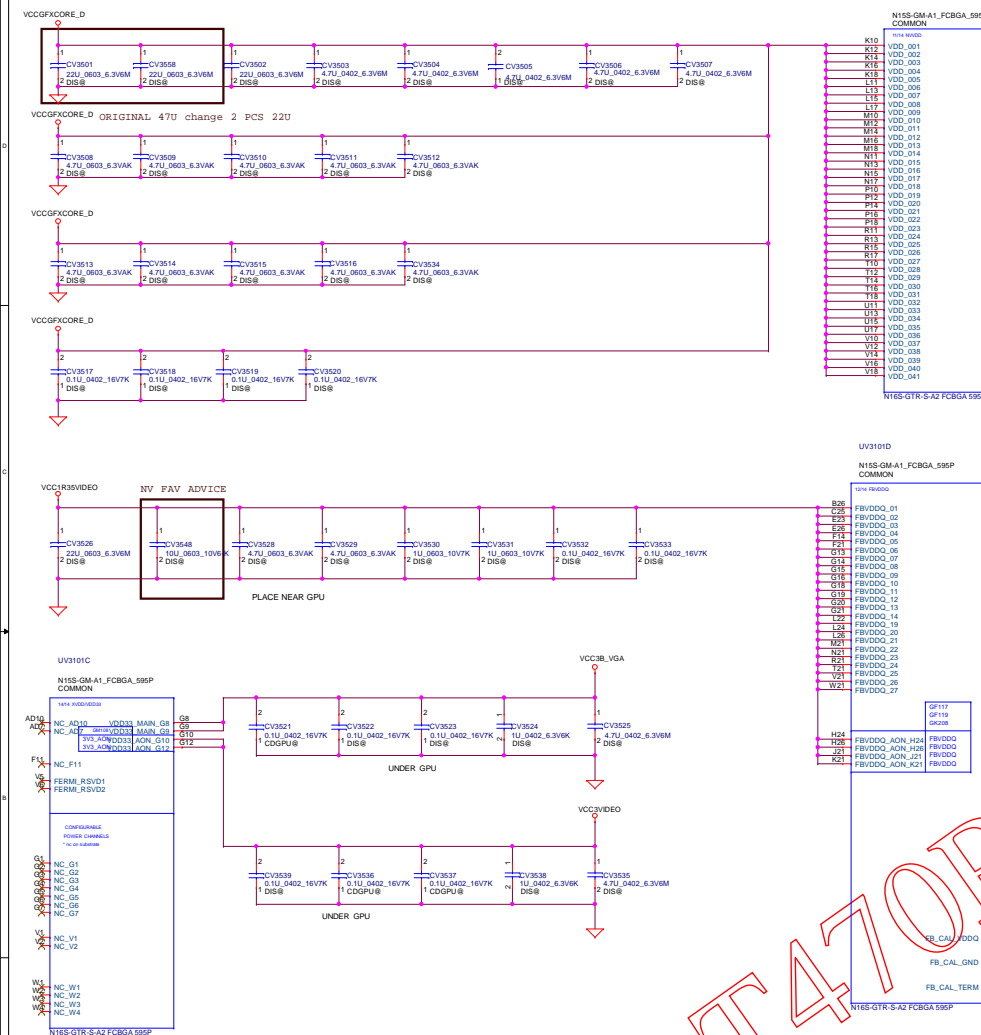
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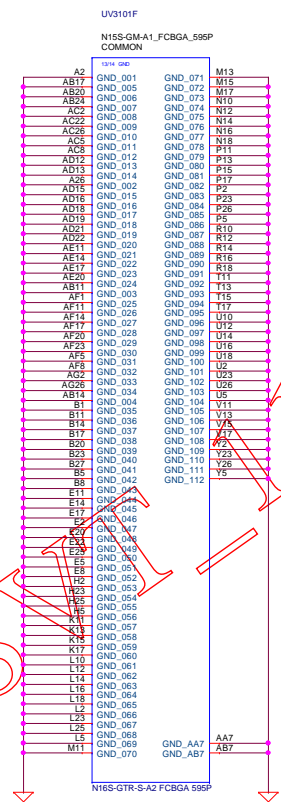
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			Doc. Drawing Number	35 of 89

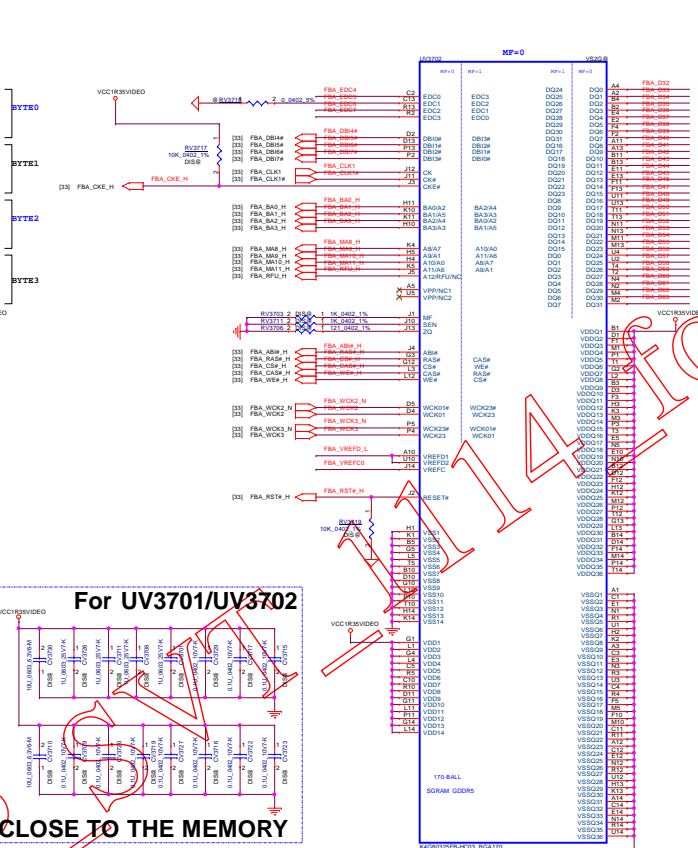
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Custom	Sheet		Rev		
Date			Sheet		
Wednesday, October 15, 2014			25 of 99		

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Date:	Wednesday, October 13, 2010			Page 37 of 39	

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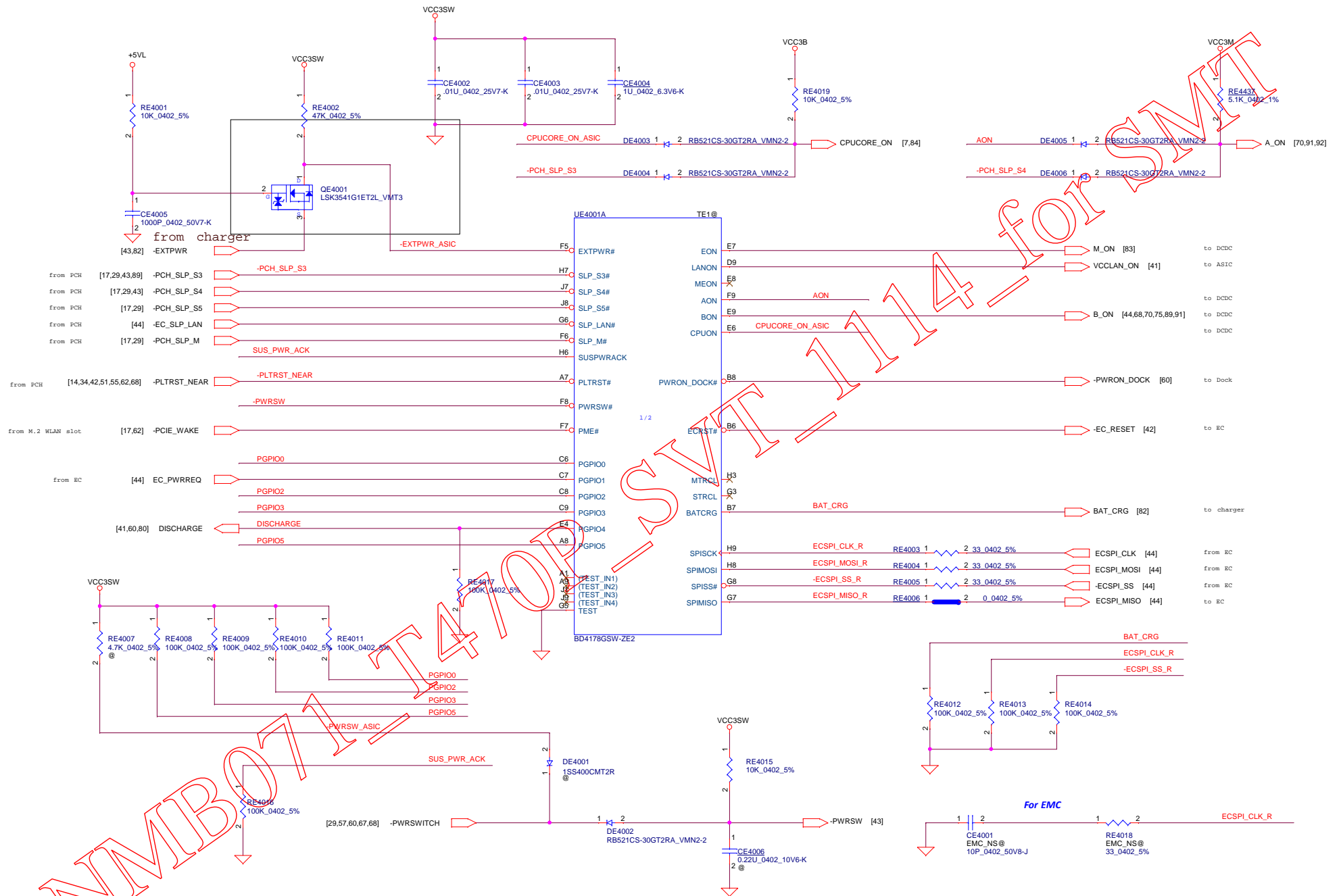
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			NTES-GT VRAM CHANNEL-A
			1114


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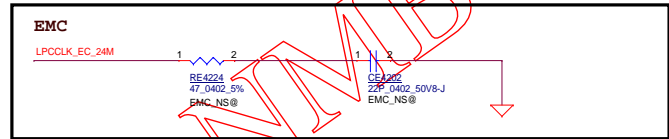
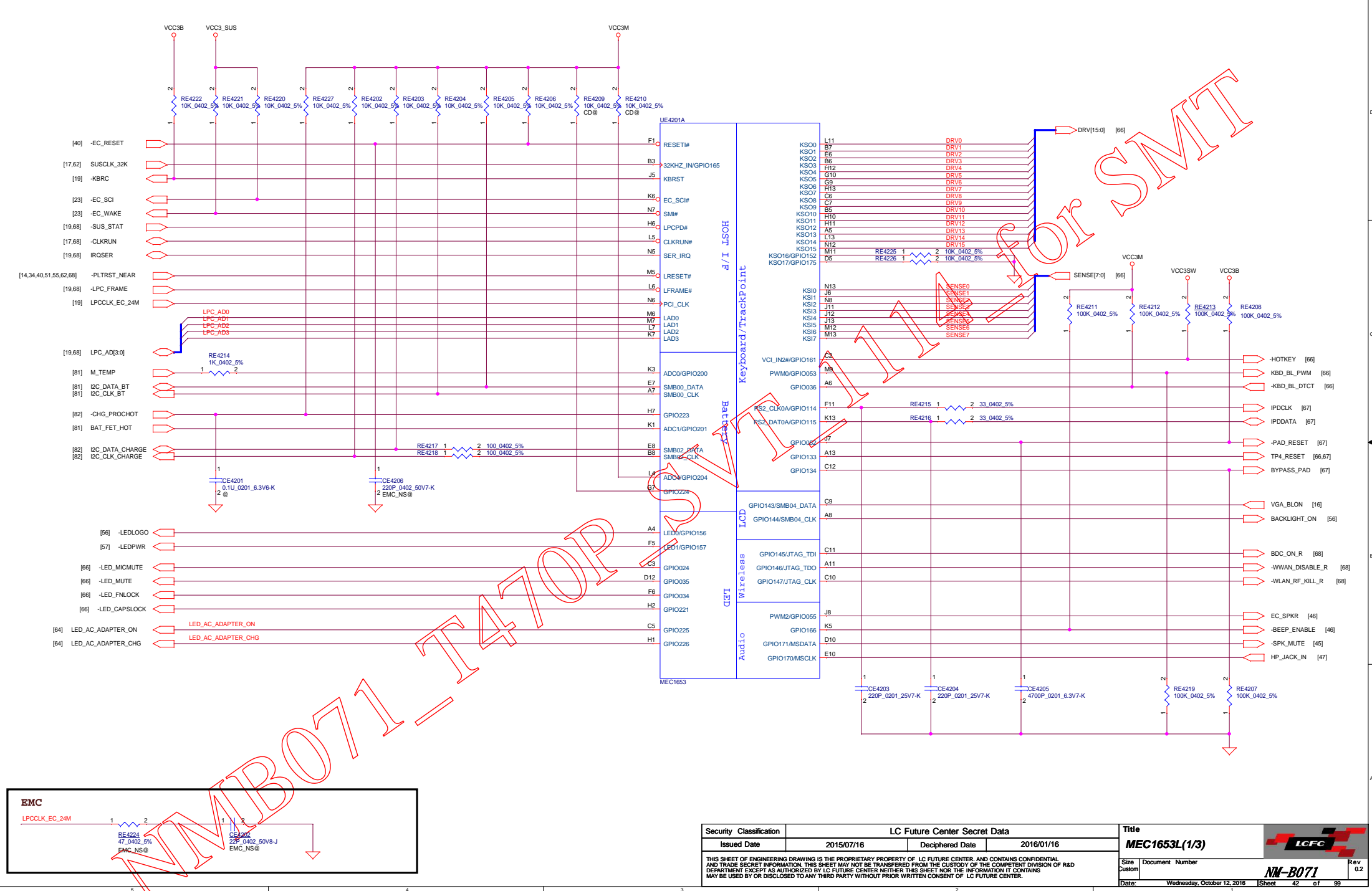
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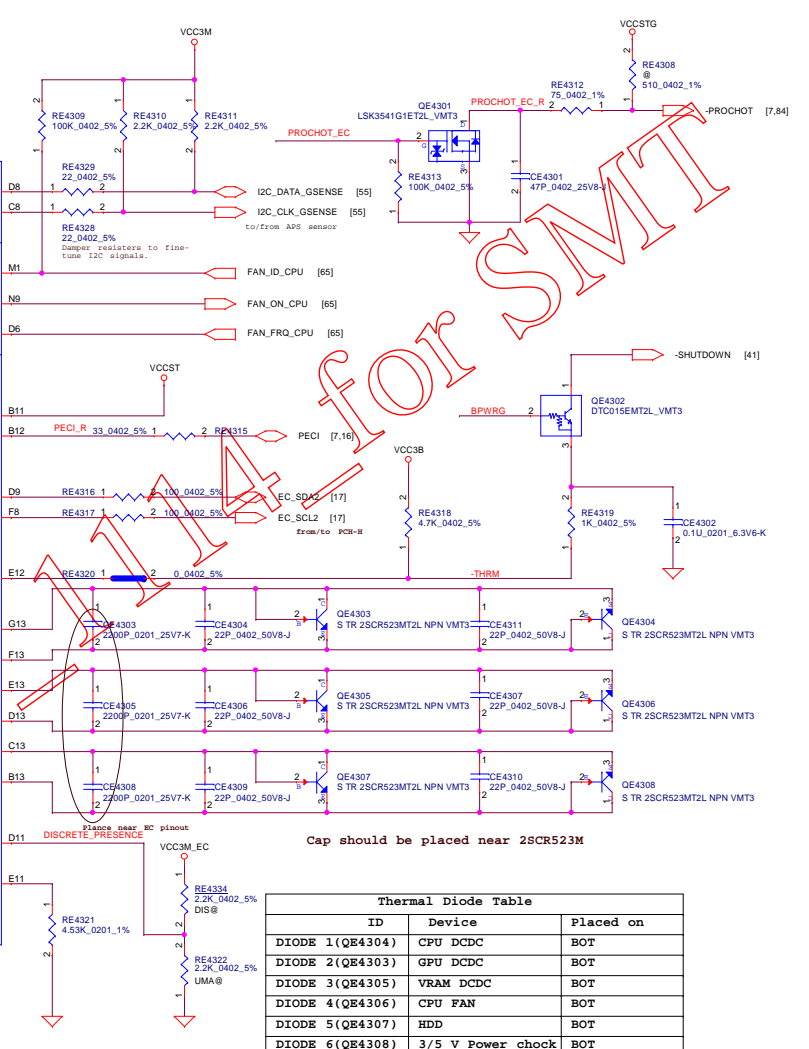
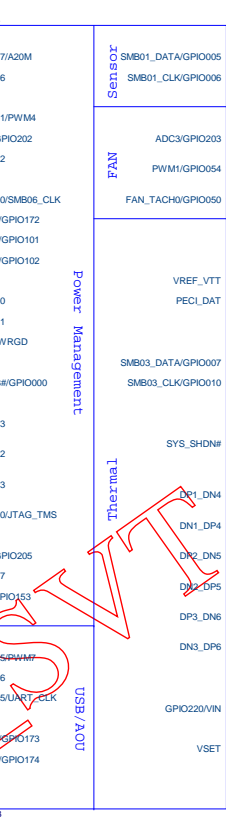
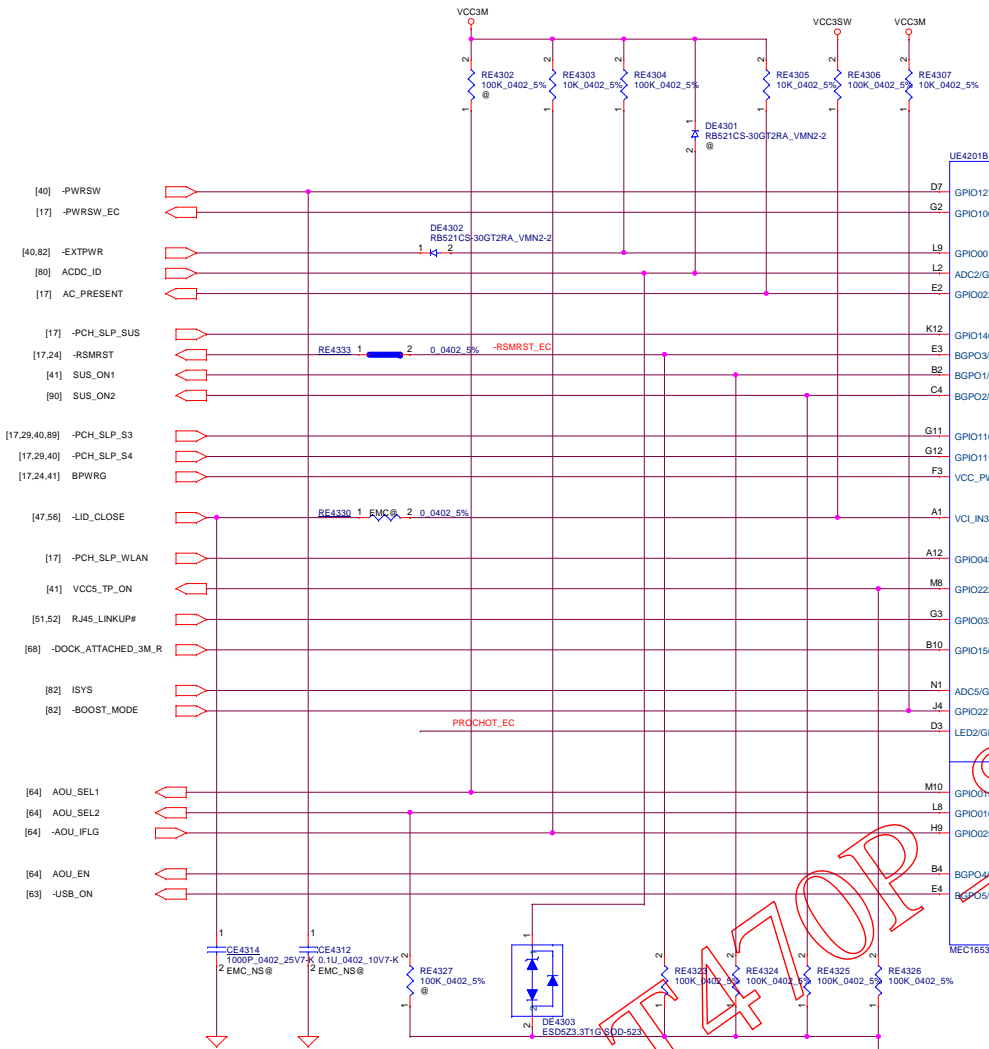
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Custom			NM-B071					
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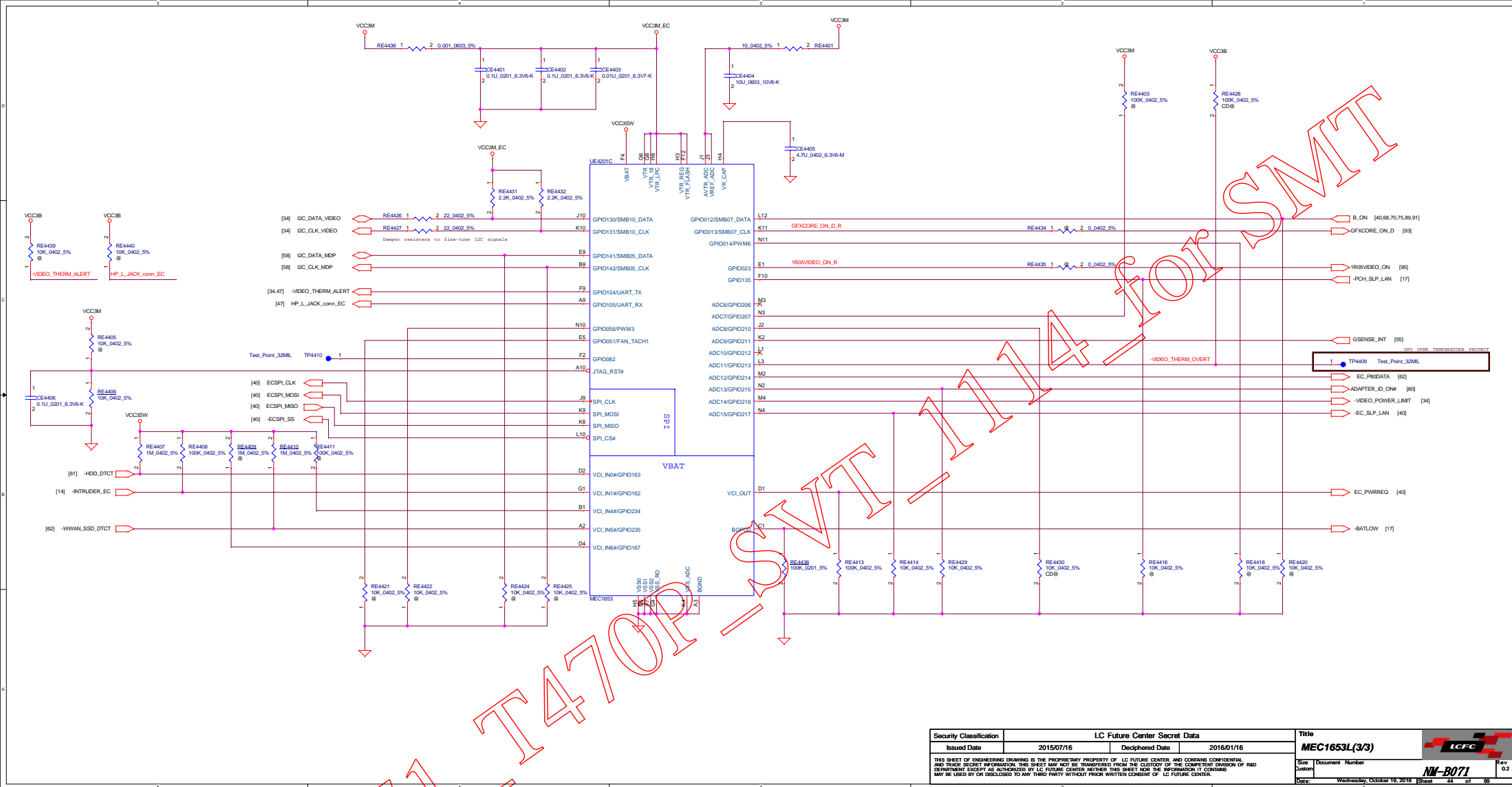


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Custom						0.2
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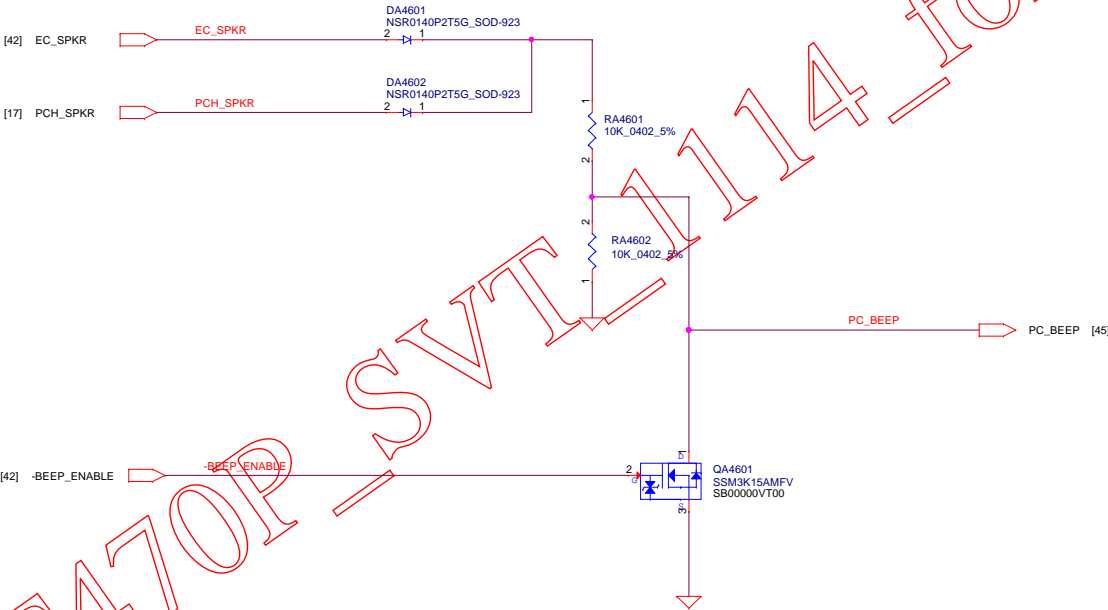


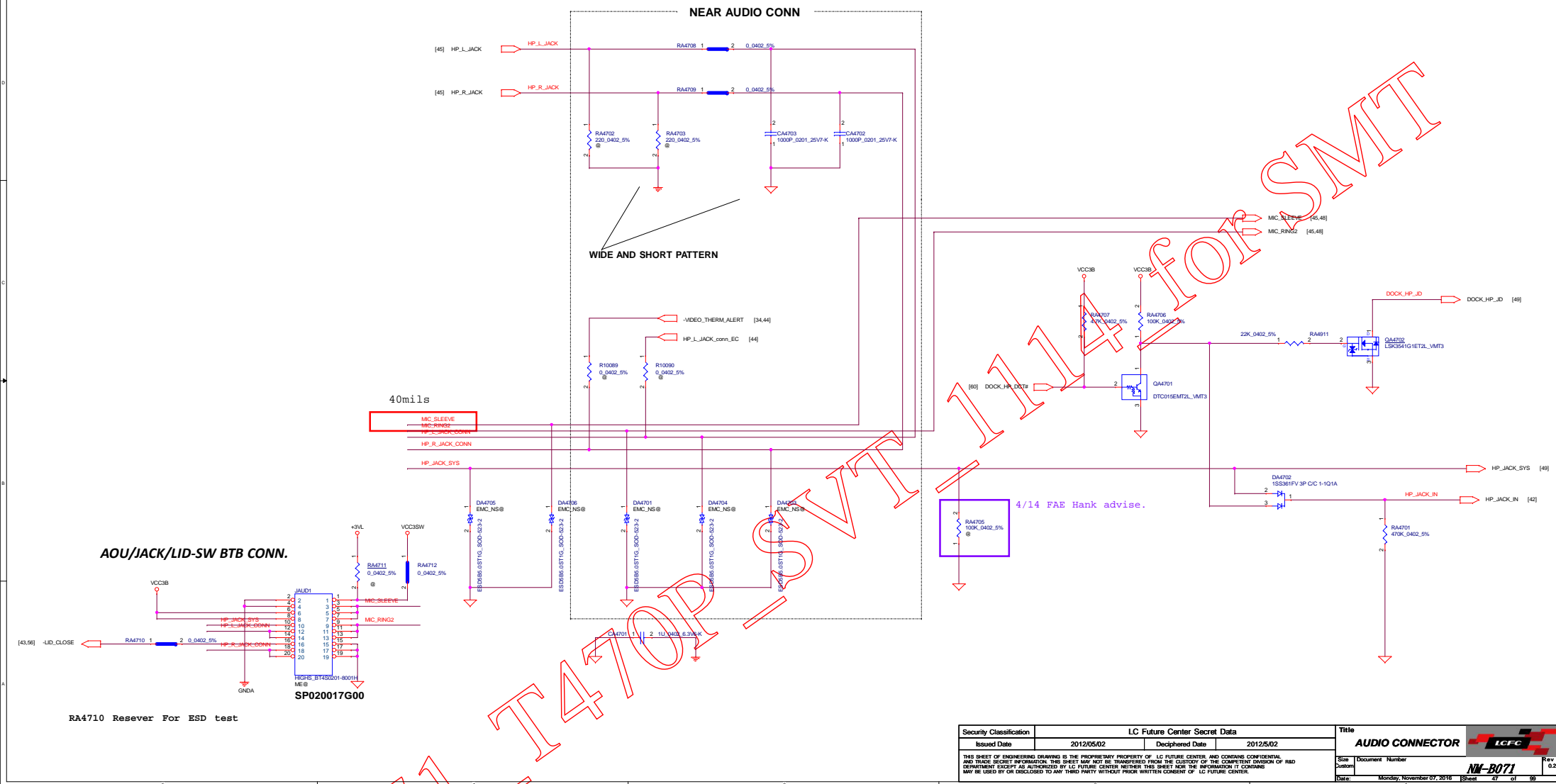
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DIODE 2(QE4303)	GPU DCDC	BOT
DIODE 3(QE4305)	VRAM DCDC	BOT
DIODE 4(QE4306)	CPU FAN	BOT
DIODE 5(QE4307)	HDD	BOT
DIODE 6(QE4308)	3/5 V Power chock	BOT

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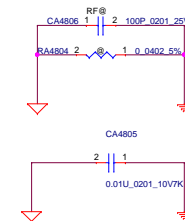
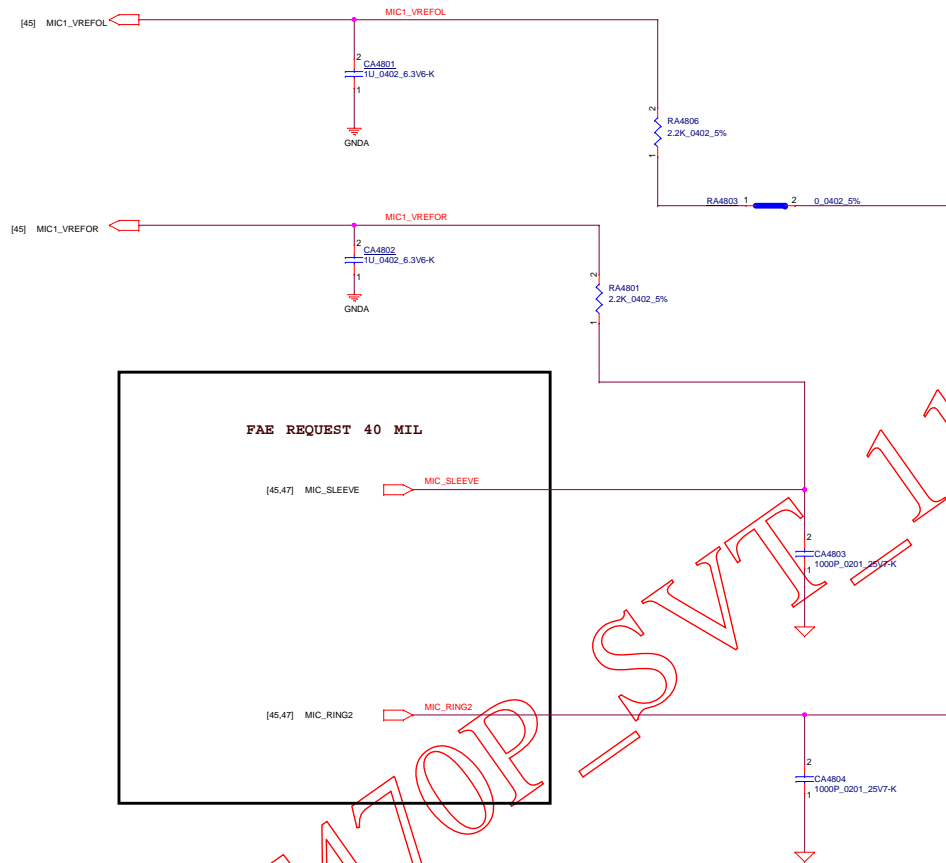


PC-BEEP





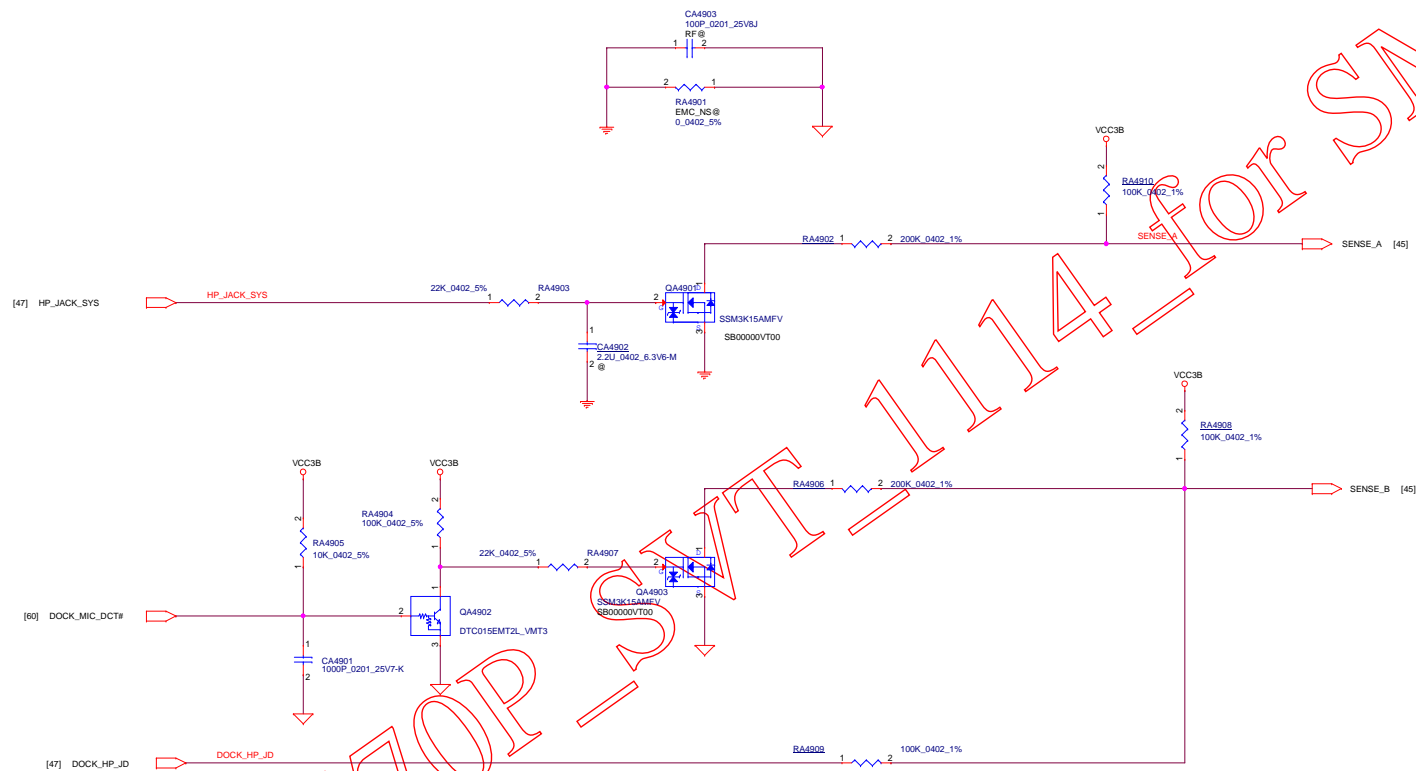
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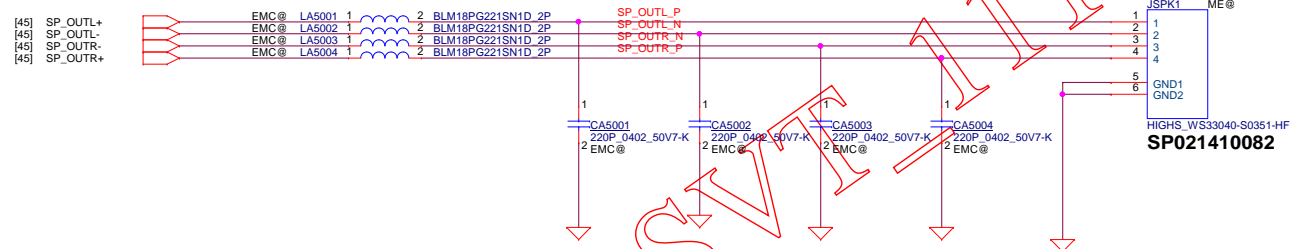





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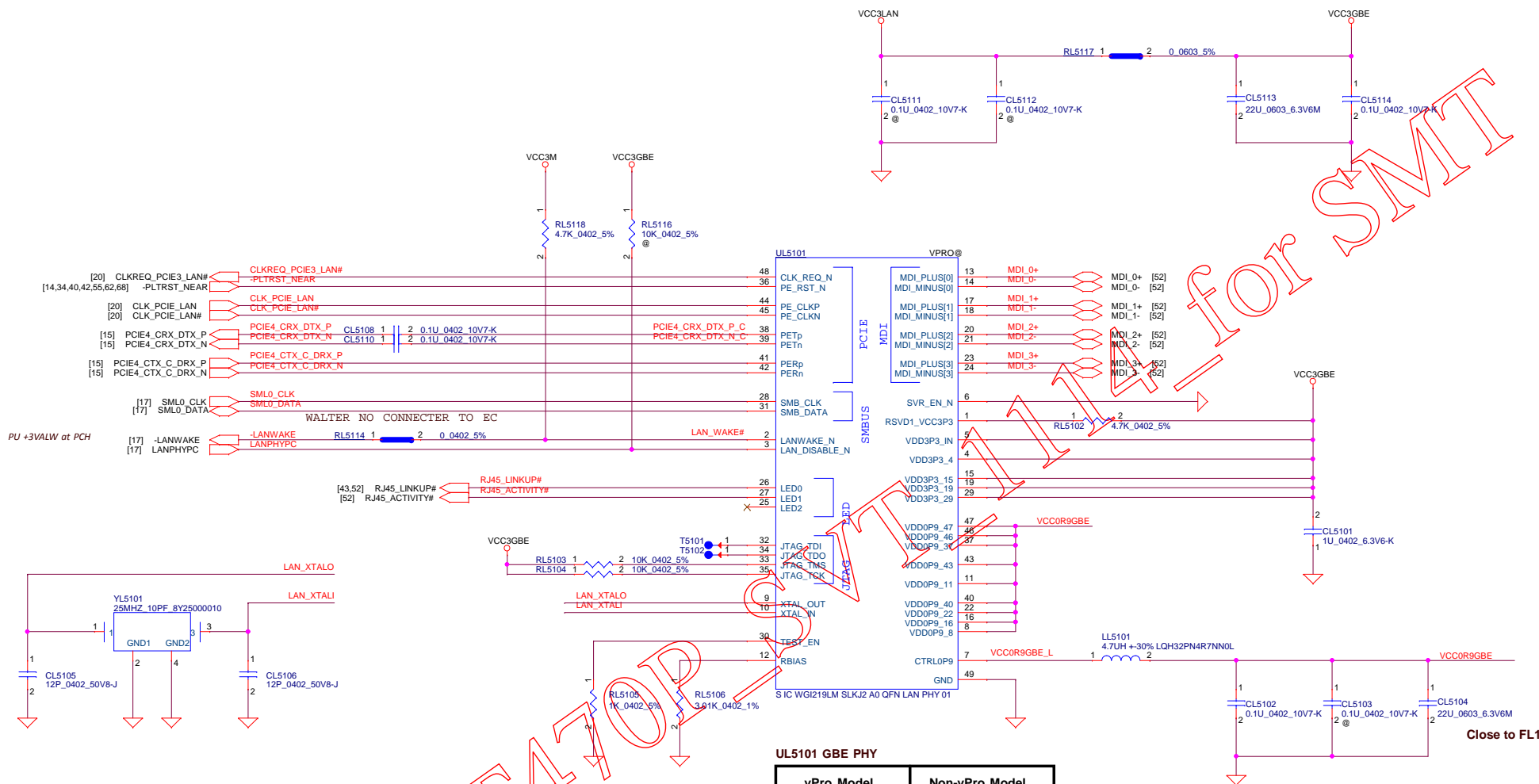
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Date: Wednesday, October 12, 2016 Sheet 49 of 99					

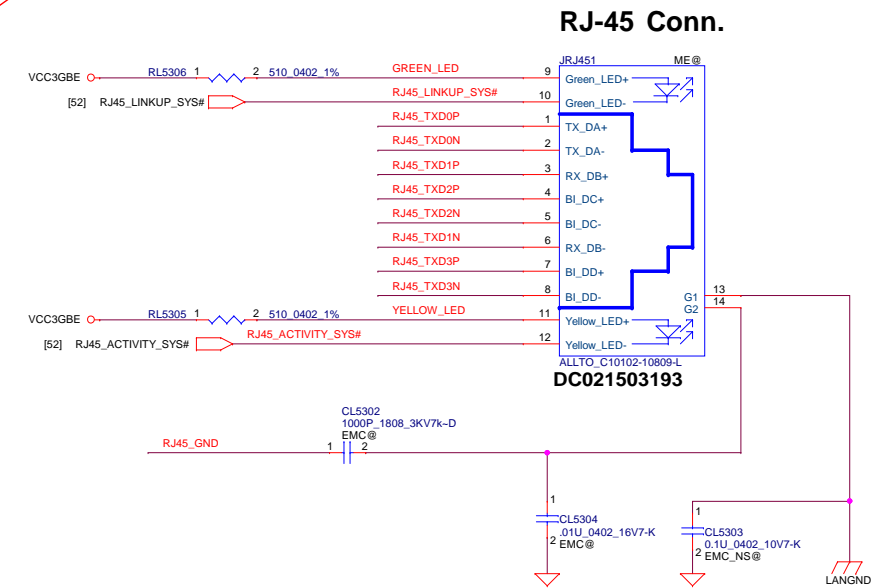
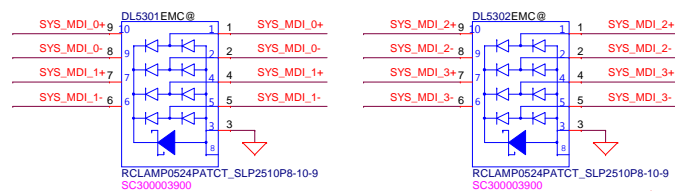
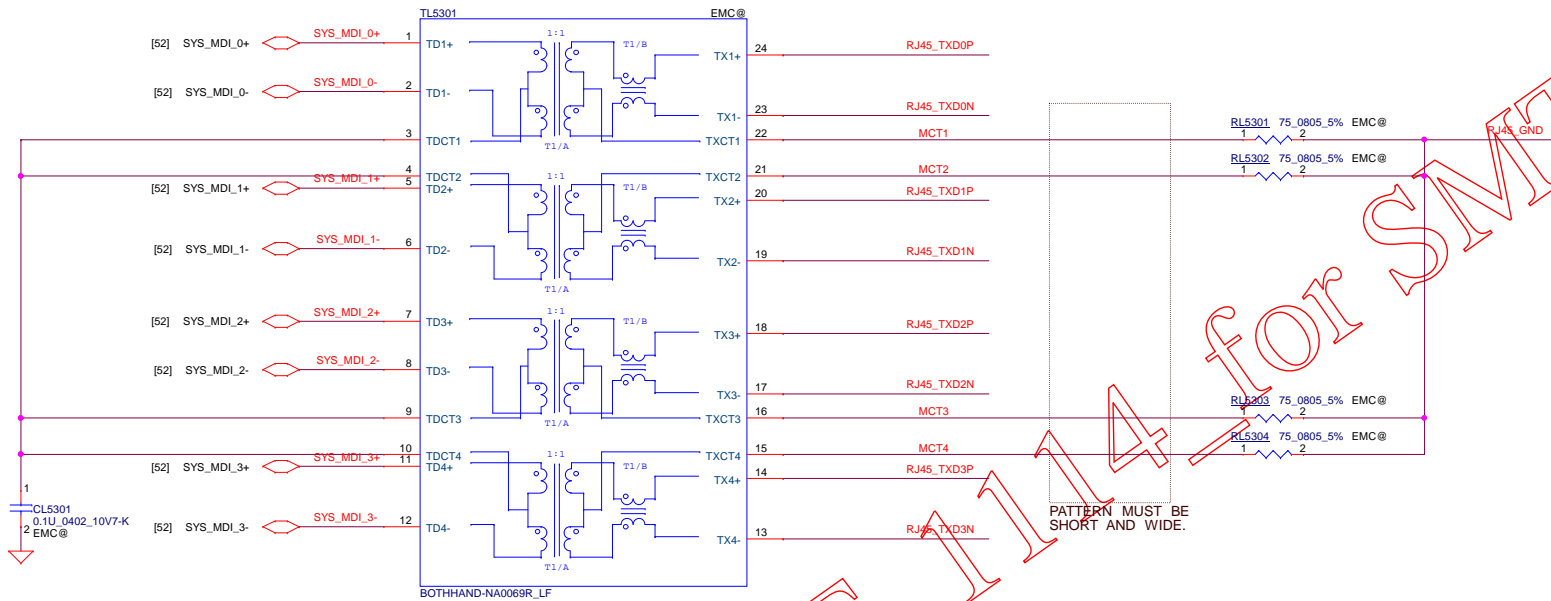
SPEAKER CONN. Speaker 4 ohm ==> 40 mils




PLACE, NEAR SPEAKER CONNECTOR

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					Custom	NM-B071	0.2
					Date:	Wednesday, October 12, 2016 Sheet 50 of 99	

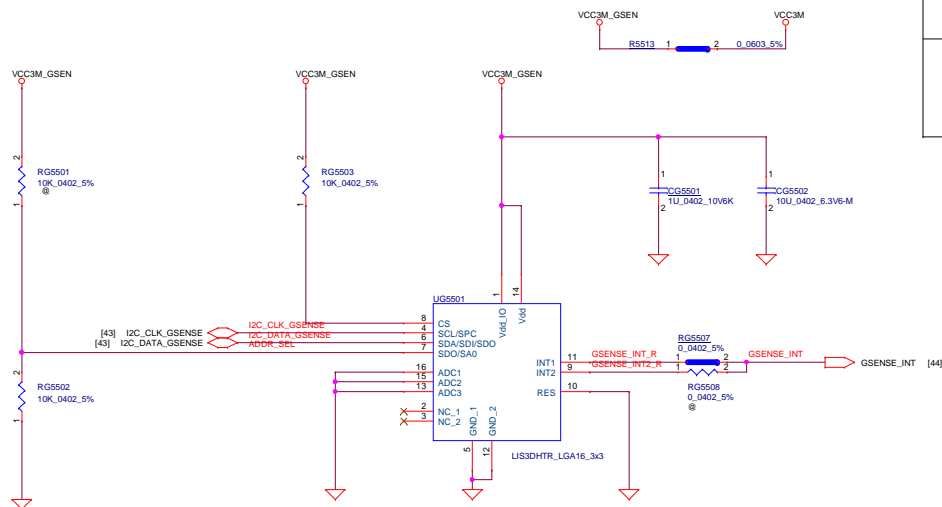




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								NM-B071	

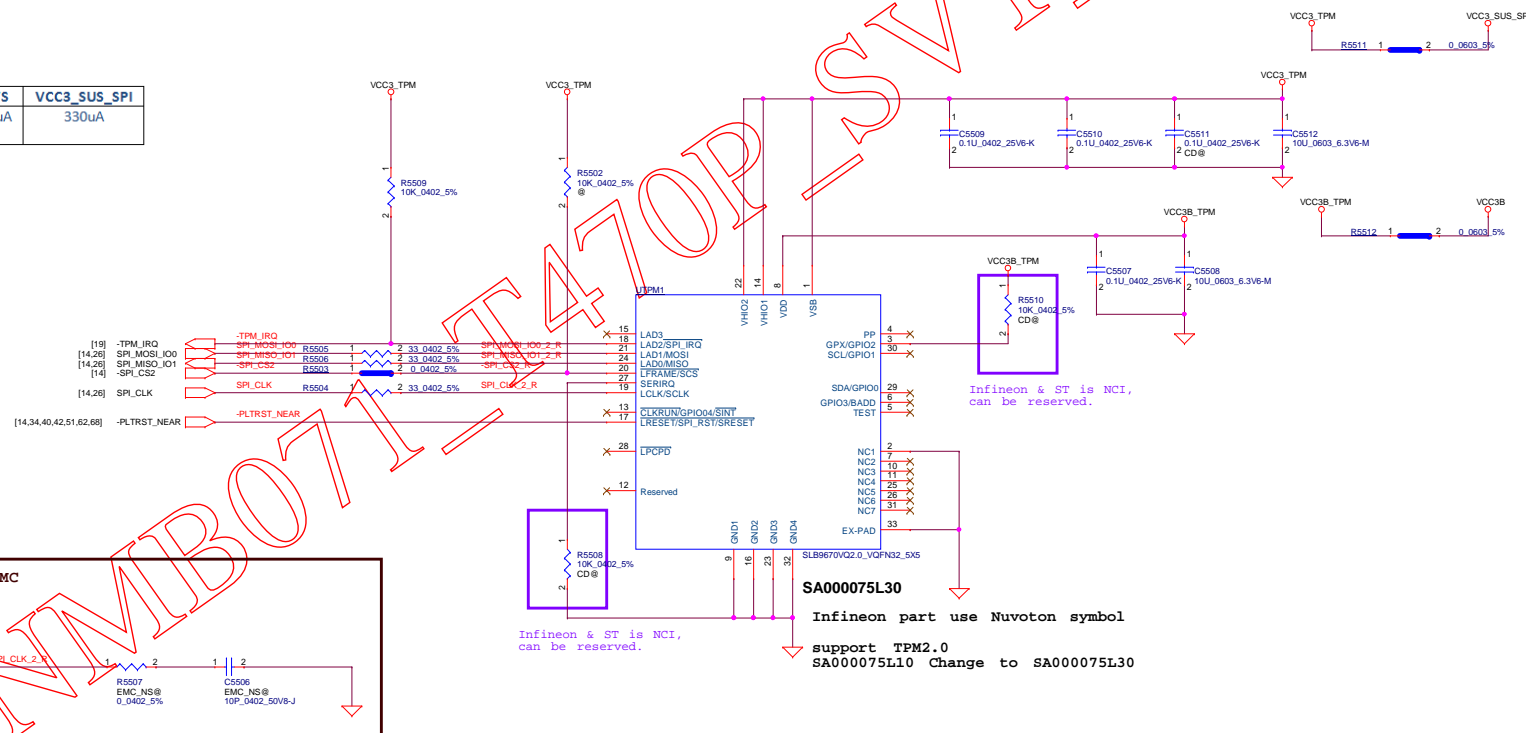
APS G-Sensor





CS	Mode Selection
H	I2C Mode
L	SPI Mode

TPM IC

TPM Pin8	+3VS	VCC3_SUS_SPI
S3~S5 current	120uA	330uA




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Title			R
G SENSOR/TPM			
Size	Document Number		R
Custom			
Date:	Wednesday, November 02, 2016 09:44		

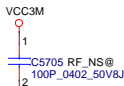
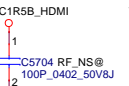
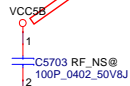
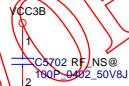
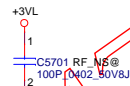
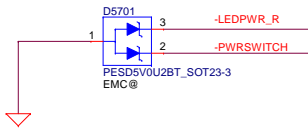
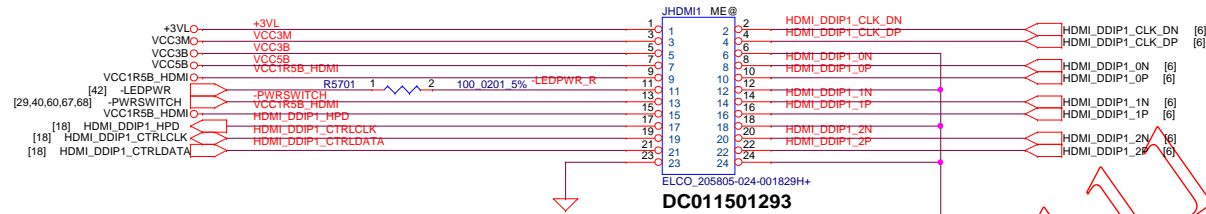
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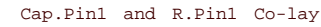


SP011408042

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				Date: Monday, November 07, 2016	Sheet 56 of 99	


M/B TO HDMI/B BTB CONN.



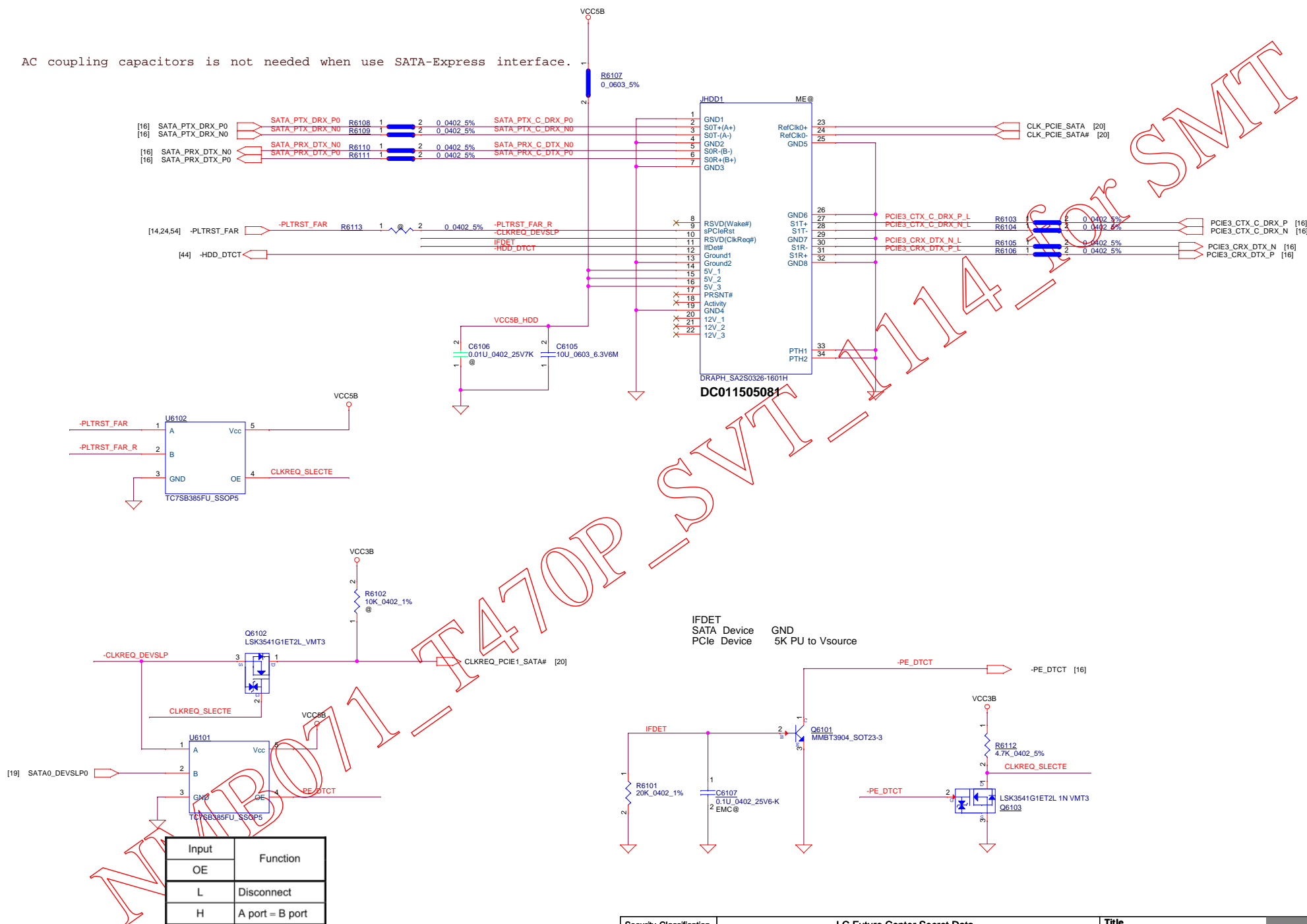


Timing diagram for MDP_ALON and MDP_ALOP signals. The diagram shows two signals, MDP_ALON and MDP_ALOP, both with a period of 0.00015s and a duty cycle of 50%. The MDP_ALON signal is high for the first half of the period and low for the second half. The MDP_ALOP signal is low for the first half of the period and high for the second half. The signals are labeled with their respective pin numbers (R5812, R5813) and the NODPRE@ signal.

DP AUX : From Repeater don't need cap, but PCH.

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Date: Wednesday, October 12, 2016				Sheet		01 of 99	

AC coupling capacitors is not needed when use SATA-Express interface.



TYPE-B NGFF SLOT FOR WWAN/SSD 3.2H CONNECTOR

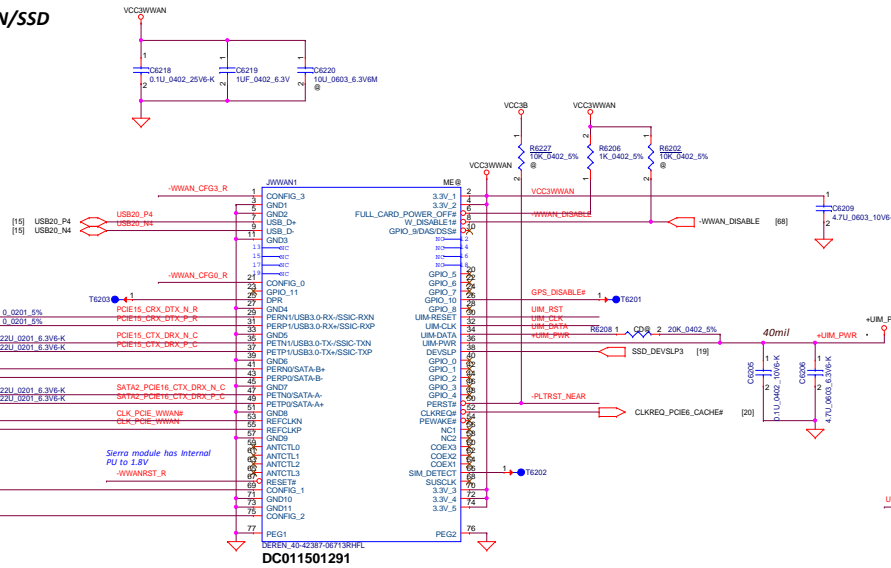
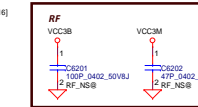
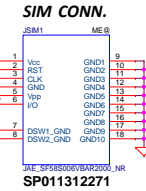
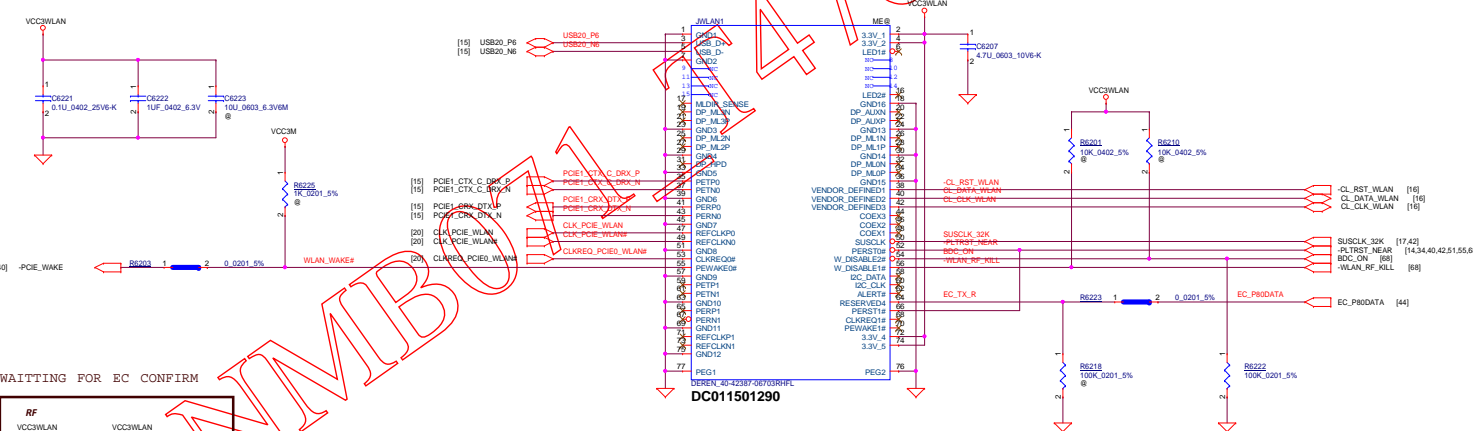


Table 27. Socket 2 Module Configuration

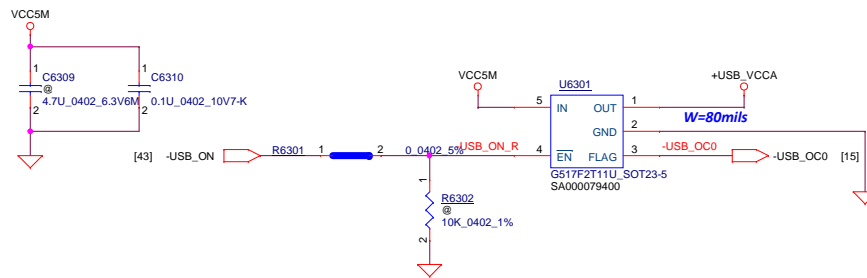
State #	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Module Type and Main Host Interface ¹	Port Configuration ²
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	NC	GND	GND	SSD – PCIe	N/A
2	GND	GND	NC	GND	WWAN – PCIe	0
3	GND	NC	NC	GND	WWAN – PCIe	1
4	GND	GND	GND	NC	WWAN – USB 3.0	0
5	GND	NC	GND	NC	WWAN – USB 3.0	1
6	GND	GND	NC	NC	WWAN – USB 3.0	2
7	GND	NC	NC	NC	WWAN – USB 3.0	3
8	NC	GND	GND	GND	WWAN – SSIC	0
9	NC	NC	GND	GND	WWAN – SSIC	1
10	NC	GND	NC	GND	WWAN – SSIC	2
11	NC	NC	NC	GND	WWAN – SSIC	3
12	NC	GND	GND	NC	WWAN – PCIe	2
13	NC	NC	GND	NC	WWAN – PCIe	3
14	NC	GND	NC	NC	RFU	N/A
15	NC	NC	NC	NC	No Module Present	N/A

¹ USB 2.0 supported on all WWAN configurations (HSIC supported on WWAN configuration 3)
² Applicable to WWAN only

TYPE-A NGFF SLOT FOR WLAN 3.2H CONNECTOR



USB POWER SWITCH

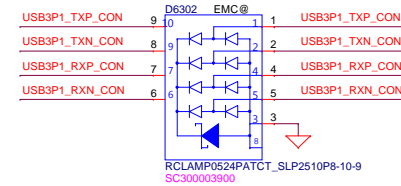
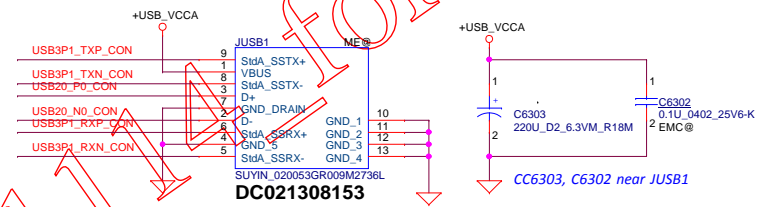
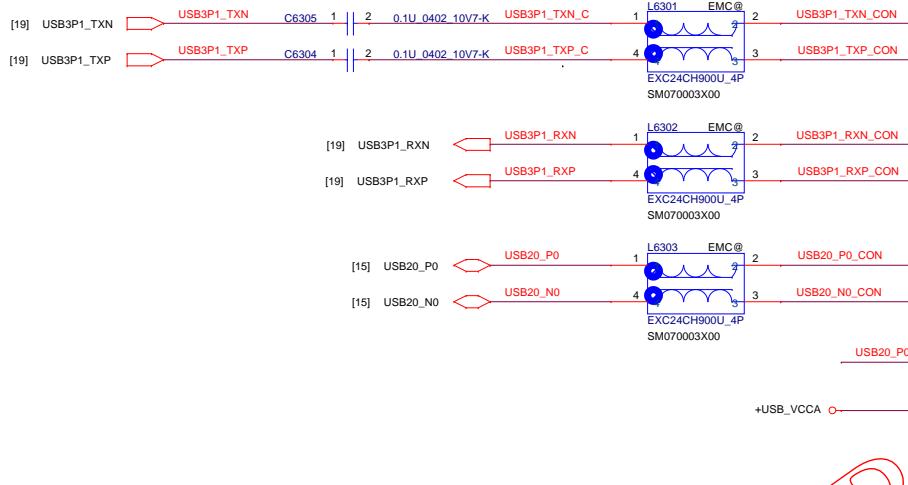


$R_{ds(on)} = 65m\Omega$
Max current continue=2.5 A

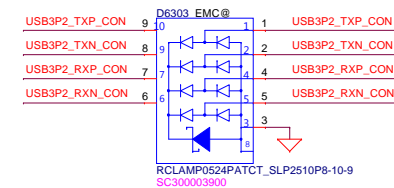
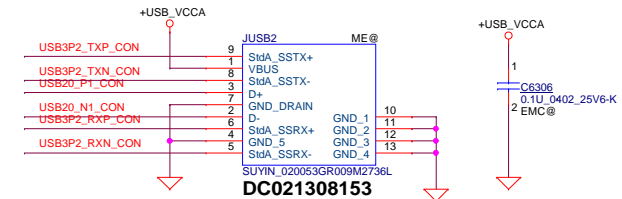
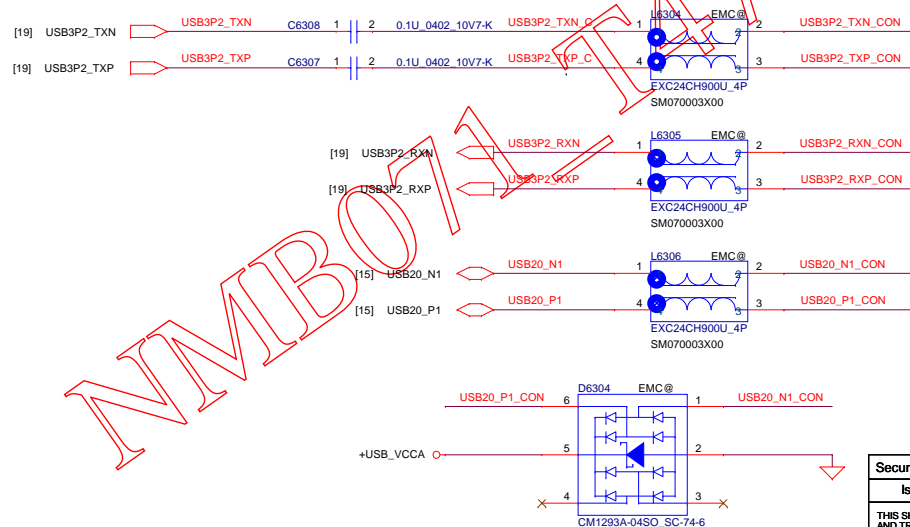
TABLE of USB3.0 Dual

GMT G517F2T11U

On Board (Right-Front)



On Board (Right-Back)



Security Classification			
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Title		
USB3 P1/2 CONN.		
Size	Document Number	Rev
Custom	NM-B071	0.2
Date: Wednesday, October 12, 2016 Sheet 63 of 99		

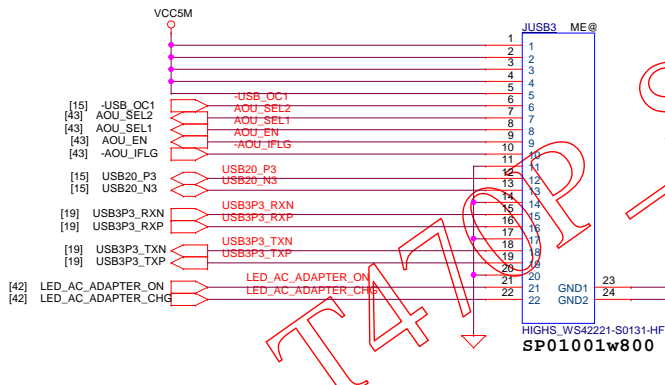
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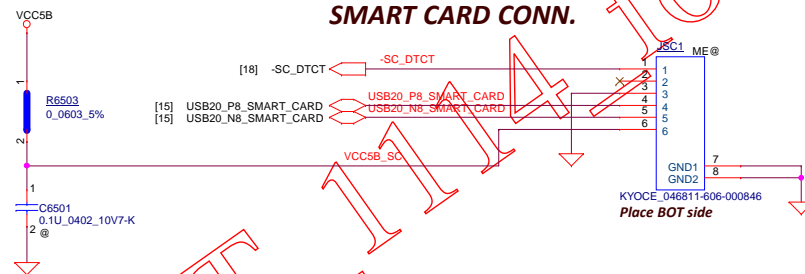
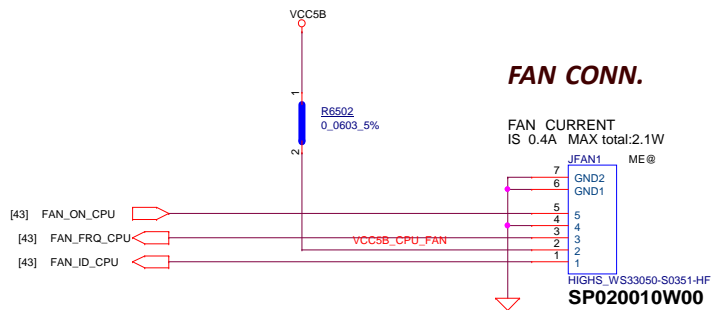
MB PIN number	MB PIN name	SB board pin name	SB PIN number
pin1-5	VCC5M	VCC5M	pin1-5
pin6	-USB_OC1	-USB_OC1	pin6
pin7	AOU_SEL2	AOU_SEL2	pin7
pin8	AOU_SEL1	AOU_SEL1	pin8
pin9	AOU_EN	AOU_EN	pin9
pin10	-AOU_IFLG	-AOU_IFLG	pin10
pin11	GND	GND	pin11
pin12	USB20_P3	USB20_P3	pin12
pin13	USB20_N3	USB20_N3	pin13
pin14	GND	GND	pin14
pin15	USB3P3_RXN	USB3P3_RXN	pin19
pin16	USB3P3_RXP	USB3P3_RXP	pin18
pin17	GND	GND	pin17
pin18	USB3P3_TXN	USB3P3_TXN	pin16
pin19	USB3P3_TXP	USB3P3_TXP	pin15
pin20	GND	GND	pin20
pin21	LED_AC_ADAPTER_ON	LED_AC_ADAPTER_ON	pin21
pin22	LED_AC_ADAPTER_CHG	LED_AC_ADAPTER_CHG	pin22


*

USB board and MB board is wire to board connector.
Due to USB board layout issue so pin define can* meet MB

USB LEFT PORT





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					Date:	Wednesday, October 12, 2016	Sheet	65 of 99

VCC3M

R6601 1 2 15K_0402_5%

R6602 1 2 15K_0402_5%

R6603 1 2 15K_0402_5%

R6604 1 2 15K_0402_5%

R6605 1 2 15K_0402_5%

R6606 1 2 15K_0402_5%

R6607 1 2 15K_0402_5%

R6608 1 2 15K_0402_5%

[42] -LED_CAPSLOCK

[42] -HOTKEY

[42] -LED_MICMUTE

[42] -LED_MUTE

[42] -LED_FNLOCK

[42] DRV[15:0]

[42] SENSE[7:0]

R6611 1 2 100_0402_5%

R6609 1 2 680_0402_5%

R6615 1 2 680_0402_5%

R6610 1 2 100_0402_5%

VCC3M_KB

DRV11

DRV8

DRV10

DRV12

DRV9

DRV13

DRV15

DRV5

DRV7

DRV6

DRV3

DRV1

DRV2

DRV4

KEYBOARD CONN.

JKB1 ME@

GND2

GND1

JAE_FL10F032HA2R3000

SP01001G400

C6605

0.1U_0201_6.3V6K

TRACK POINT CONN.

VCC5_TP

R6612 4.7K_0402_5%

R6613 4.7K_0402_5%

VCC5_TP

R6614 15K_0402_5%

VCC5_TP

C6601

0.1U_0201_6.3V6K

VCC5B

[42] -KBD_BL_DTCT

[42] KBD_BL_PWM

[67] TP4CLK

[42.67] TP4_RESET

[67] TP4DATA

R6617 1 2 0_0201_5%

R6618 1 2 0_0201_5%

JTP1 ME@

GND2

GND1

JAE_FL10F012HA1R3000

SP01001G300

C6606

1000P_0402_25V7-K

2 EMC_NS@

C6604

220P_0201_25V7K

C6602

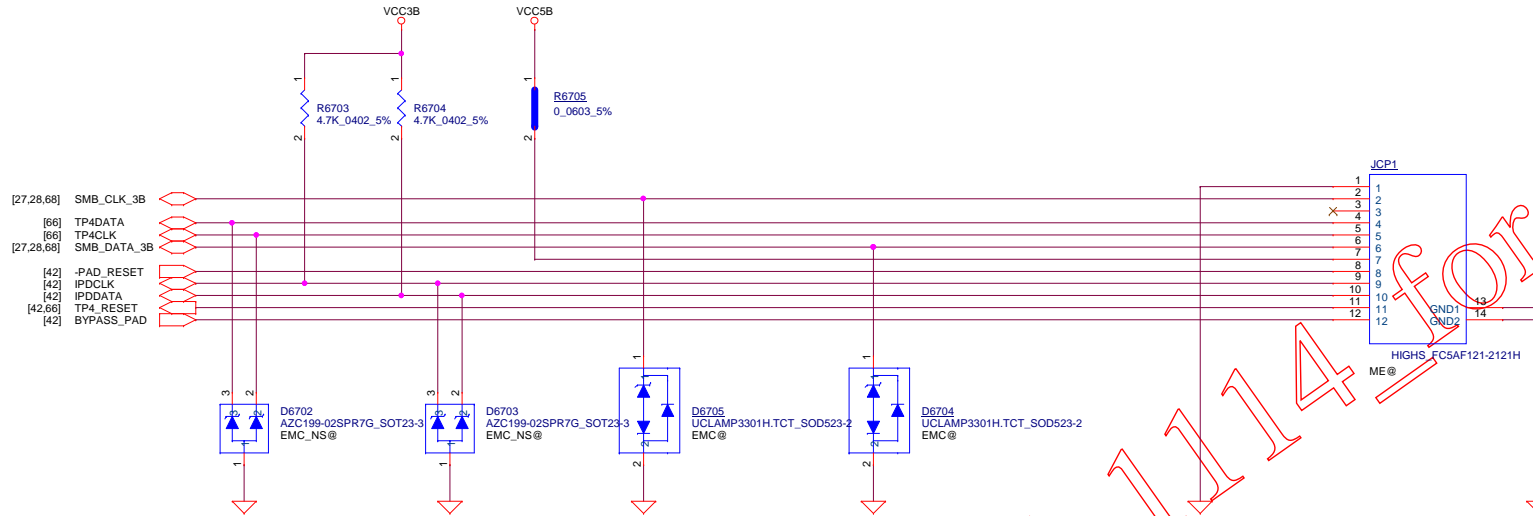
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C6603

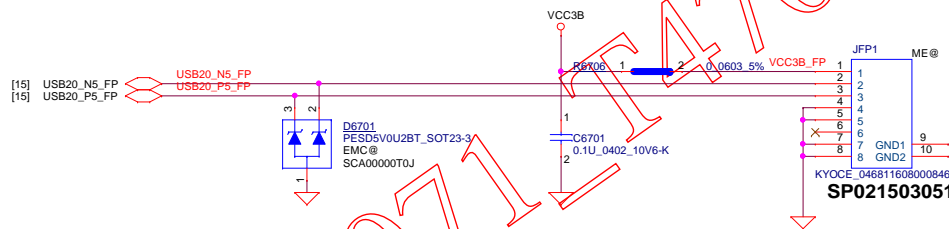
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				Date:	Monday, November 07, 2016	Sheet 66 of 99

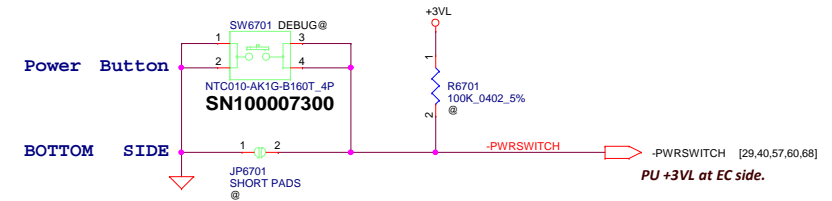
Click Pad




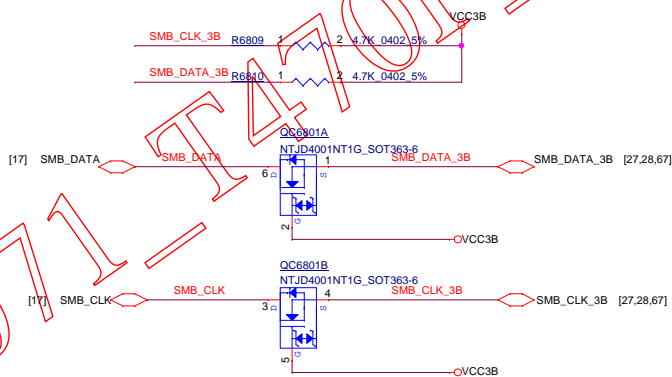
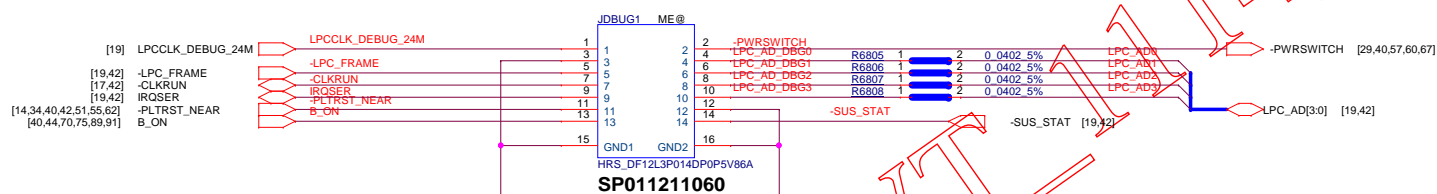
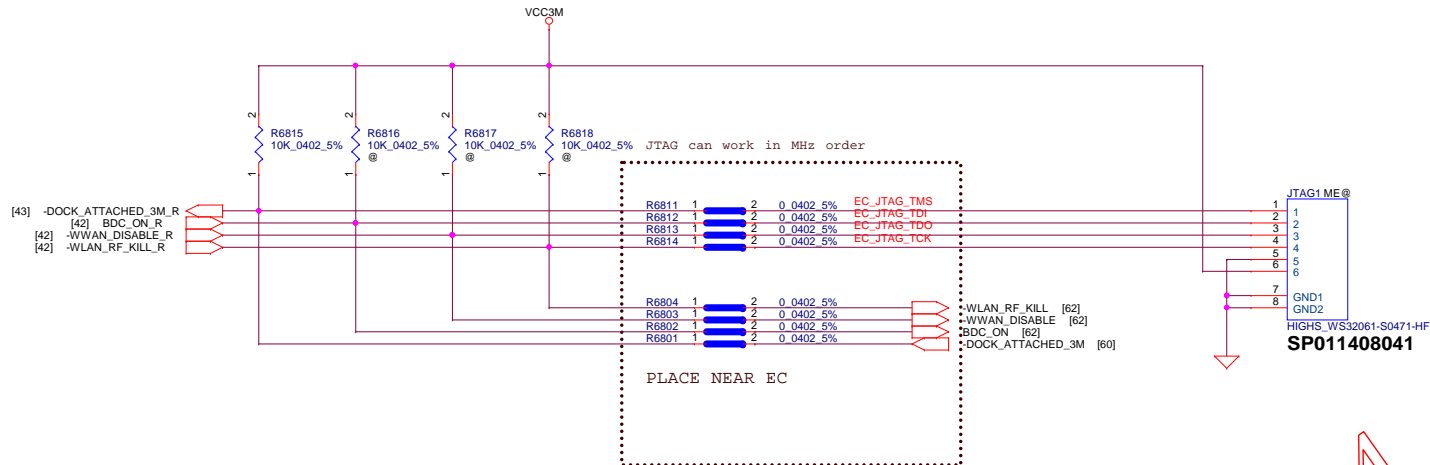
FingerPrint CONN.



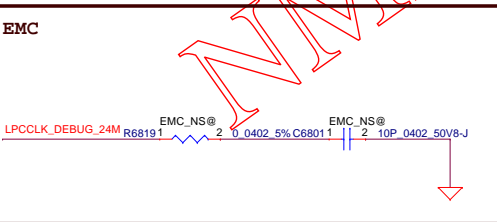
PWRBTN FOR DEBUG



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Non ECSL part Change
SB00000EO1J=>SB00000YN00

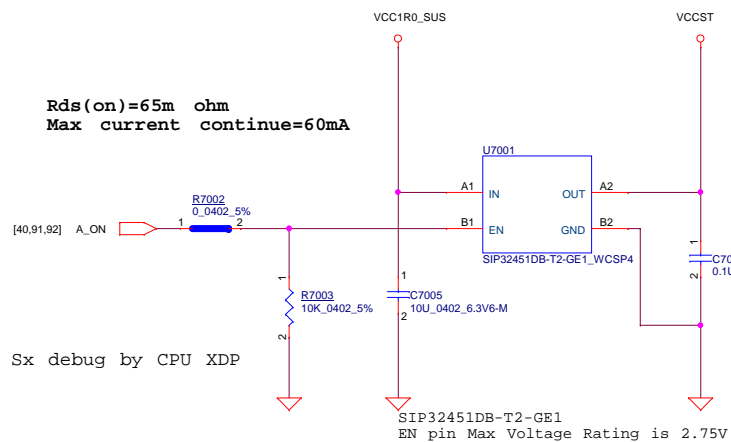


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				Rev	0.2

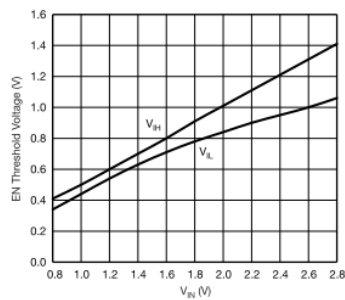
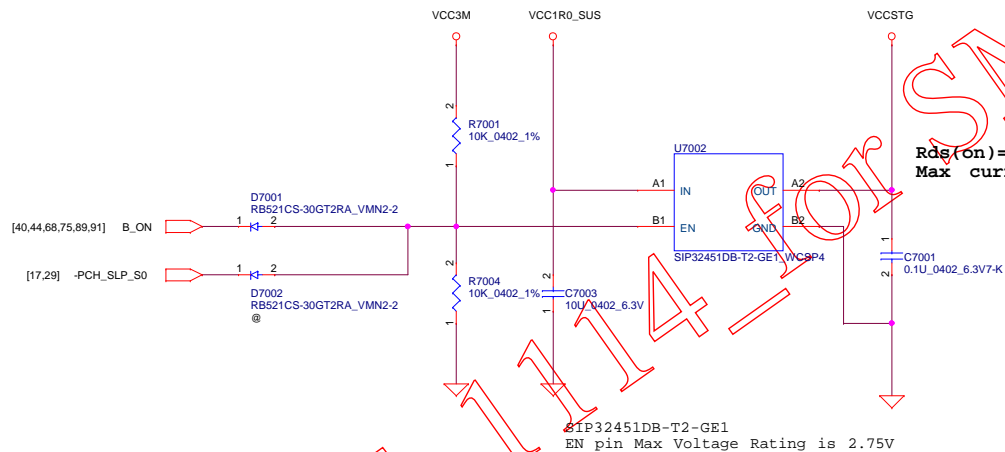
NMIB071-T470P-SVT-1114_for SMT

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				Date: Wednesday, October 12, 2016		Sheet 69 of 99

$R_{ds(on)}=65m\ \Omega$
Max current continue=60mA

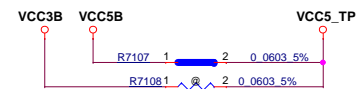
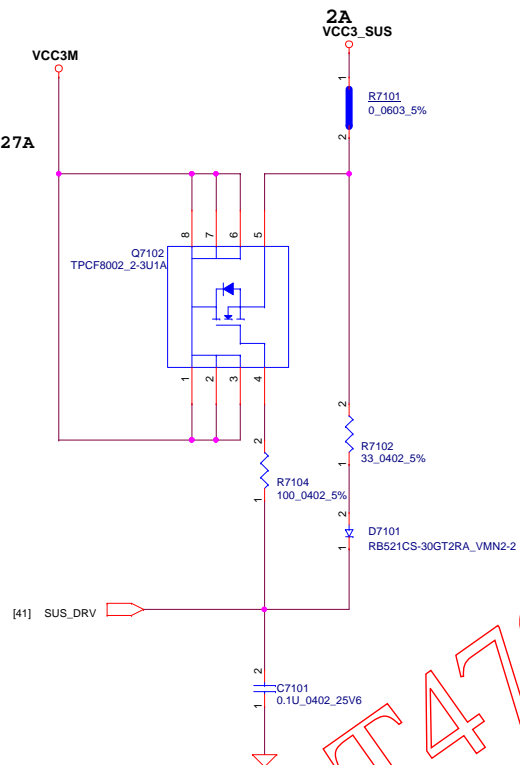


$R_{ds(on)}=65m\ \Omega$
Max current continue=60mA




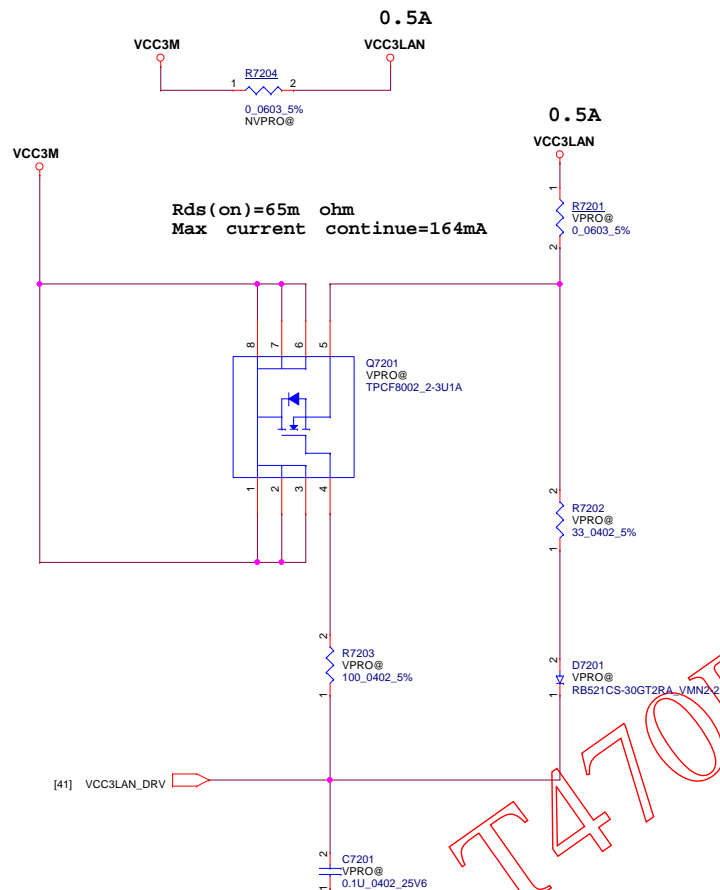
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Issued Date	2014/07/01	Deciphered Date	2015/12/31	Size	Document Number	Custom		Rev	0.2
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								Date:	Wednesday, October 12, 2016 Sheet 70 of 99

Rds(on)=65m ohm
Max current continue=4.27A



Rds(on)=371m ohm
Max current continue=15mA

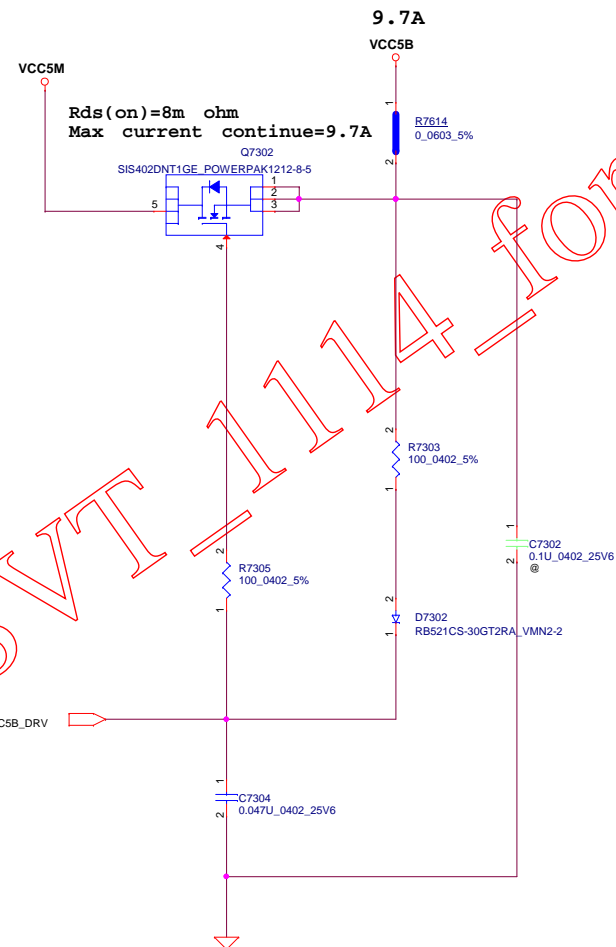
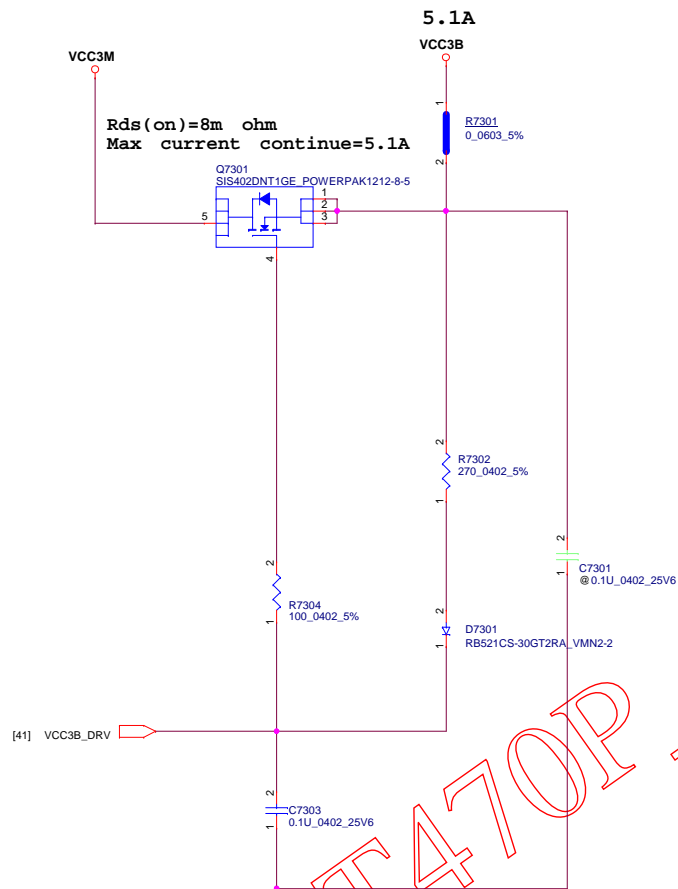
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						Custom	NM-B071		
Date:						Wednesday, October 12, 2016 Sheet 71 of 99			




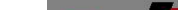
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				Sheet	72 of 99

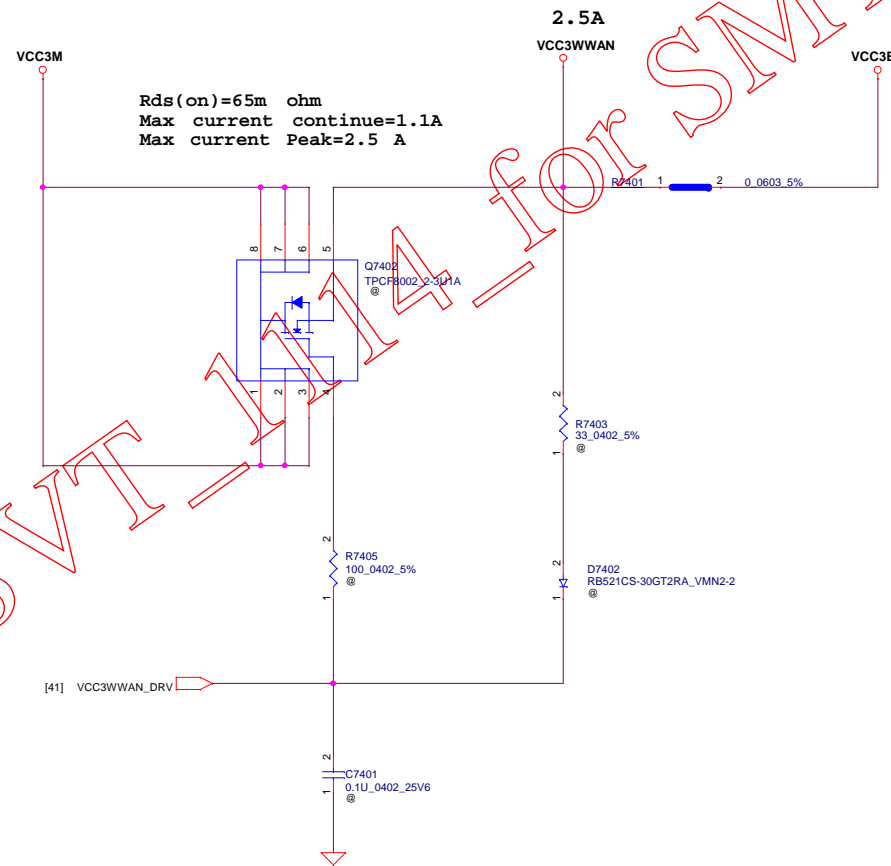
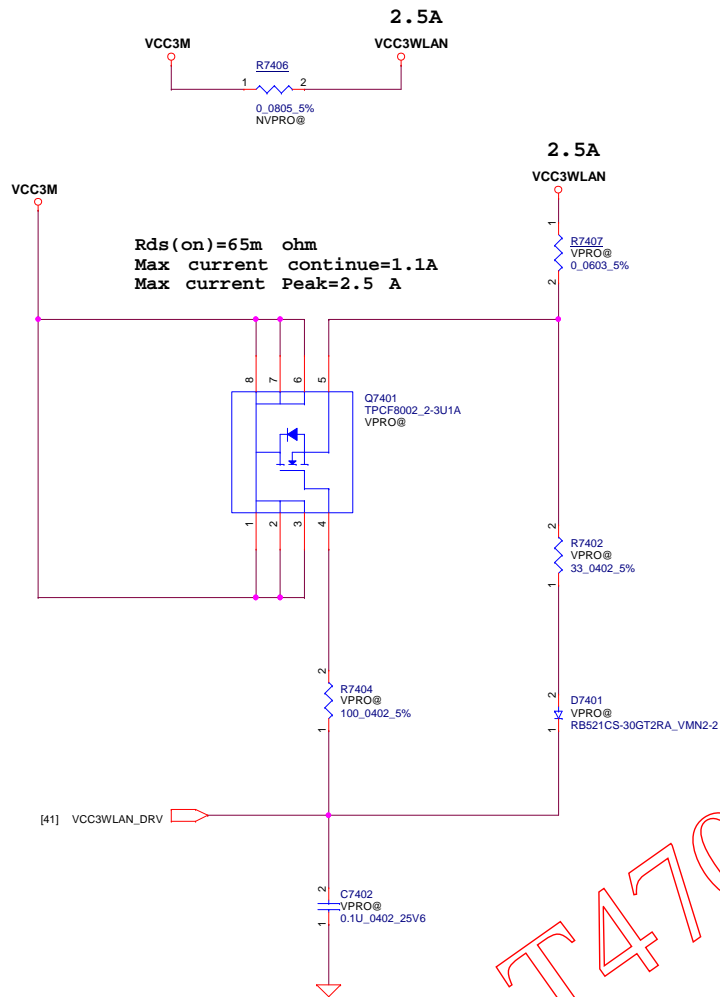


Rev 0.2



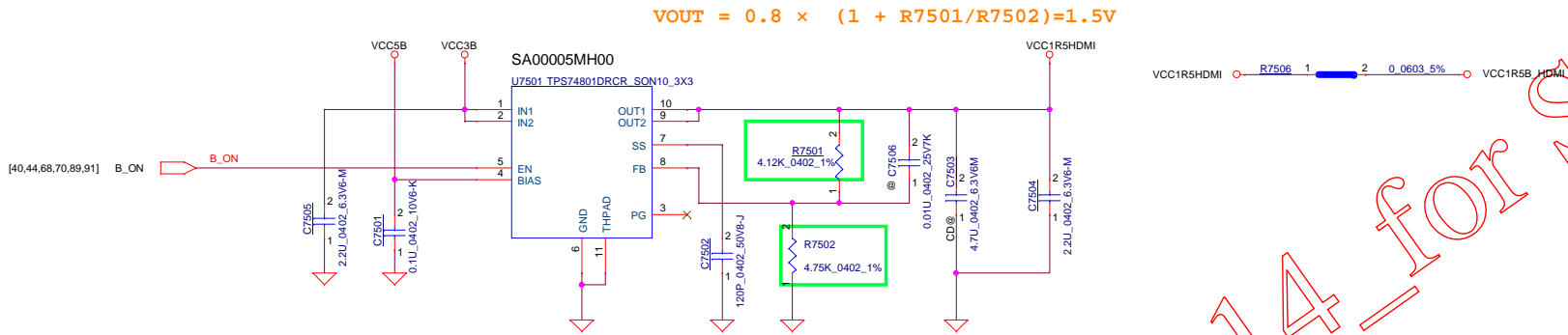
NMB071-T470P

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Issued Date	2014/07/01	Deciphered Date	2015/12/31	LOAD SW B		
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				Date:	Wednesday, October 12, 2016	Rev 0.2
				Sheet	73 of 99	

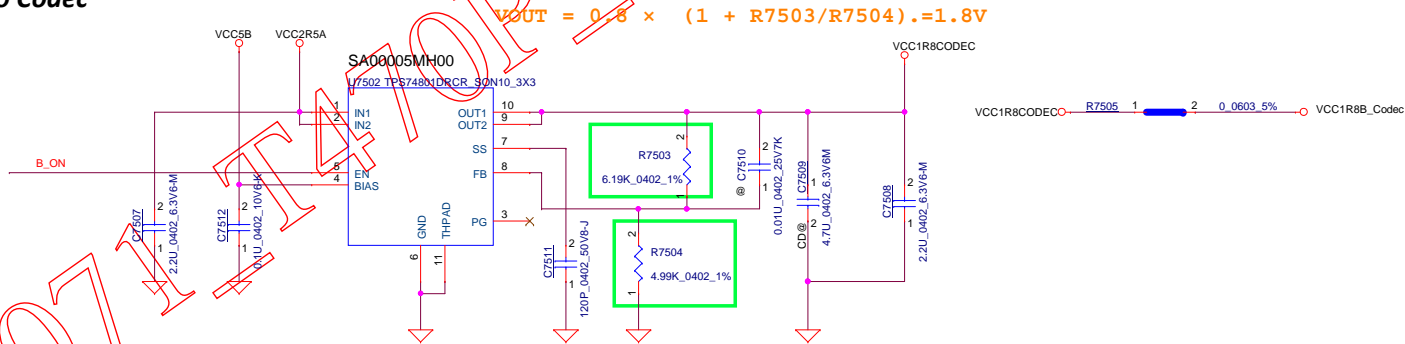


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Issued Date	2014/07/01	Deciphered Date	2015/12/31	LOAD SW WWAN&WLAN	
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				Date:	Wednesday, October 12, 2016
				Sheet	74 of 99
				Rev	0.2

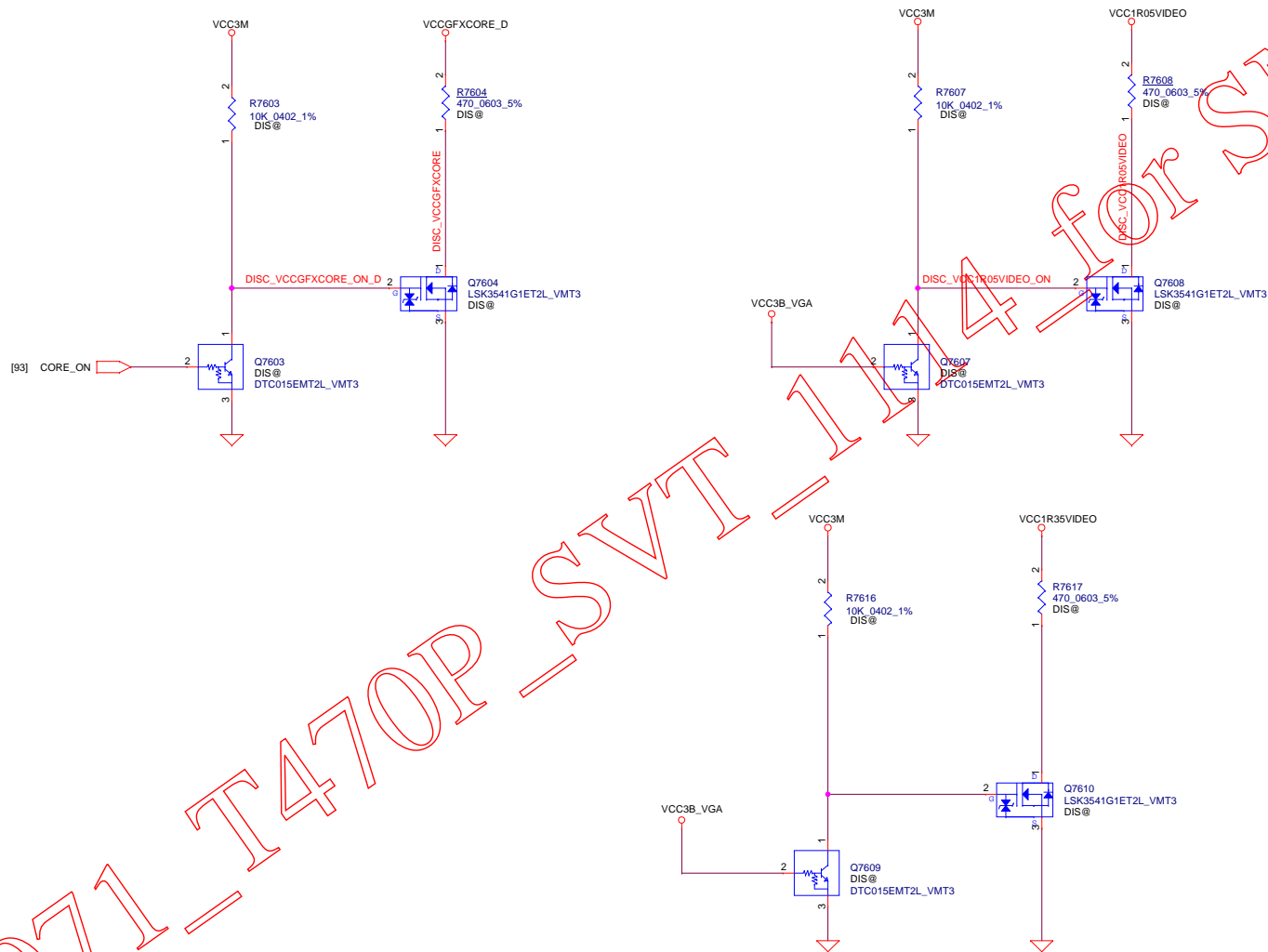
VCC3B transform 1.5V to HDMI



VCC2R5A transform 1.8V to Codec




NMIB071-T470P-SVT-1114 for SMT



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2014/07/01	Deciphered Date	2015/12/31	DISCHARGE CIRCUIT VIDEO	
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				Date:	Wednesday, October 12, 2016
				Sheet	76 of 99
				Rev	0.2

NMB071-T470P-SVT-1114_for SMT

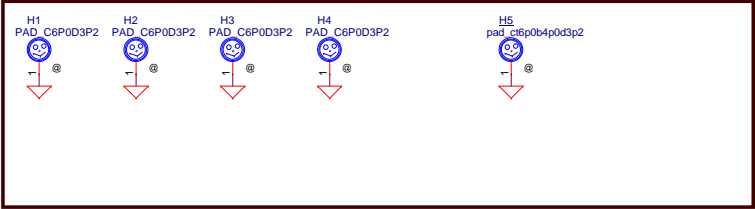
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				Custom	NM-B071	0.2	
Date:				Wednesday, October 12, 2016 Sheet 77 of 99			

Debug connector

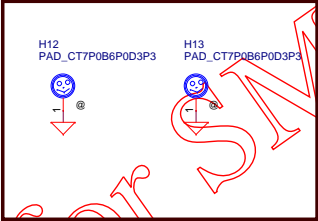
BIOS ROM socket	S SOCKET ACES 50960-0084N-001 BIOS ROM	J2601	LTCX0049G00
BIOS debug conn	S H-CONN HIROSE DF12L(3.0)-14DP-0.5V(86)	JDEBUG1	SP01001H10T
EC debug conn	S H-CONN HIGHSTAR WS32061-S0471-HF P1.25	JTAG1	SP01001VA00
Power botton in MB	S TACT SW NTC010-AK1G-B160T SPST H3.1 4P	SW6701	SN100007300
SW/ME debug conn	FCI_10051922-1810ELF Kyocera 04-6809- 618-220-846+	J2901	

Screw Hole

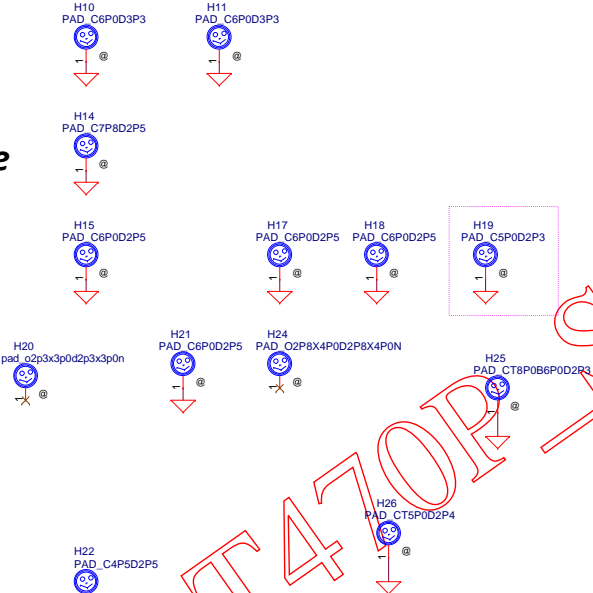
For CPU and GPU



AUDIO SCREW

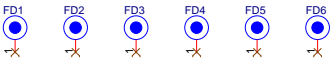



For ME GND hole

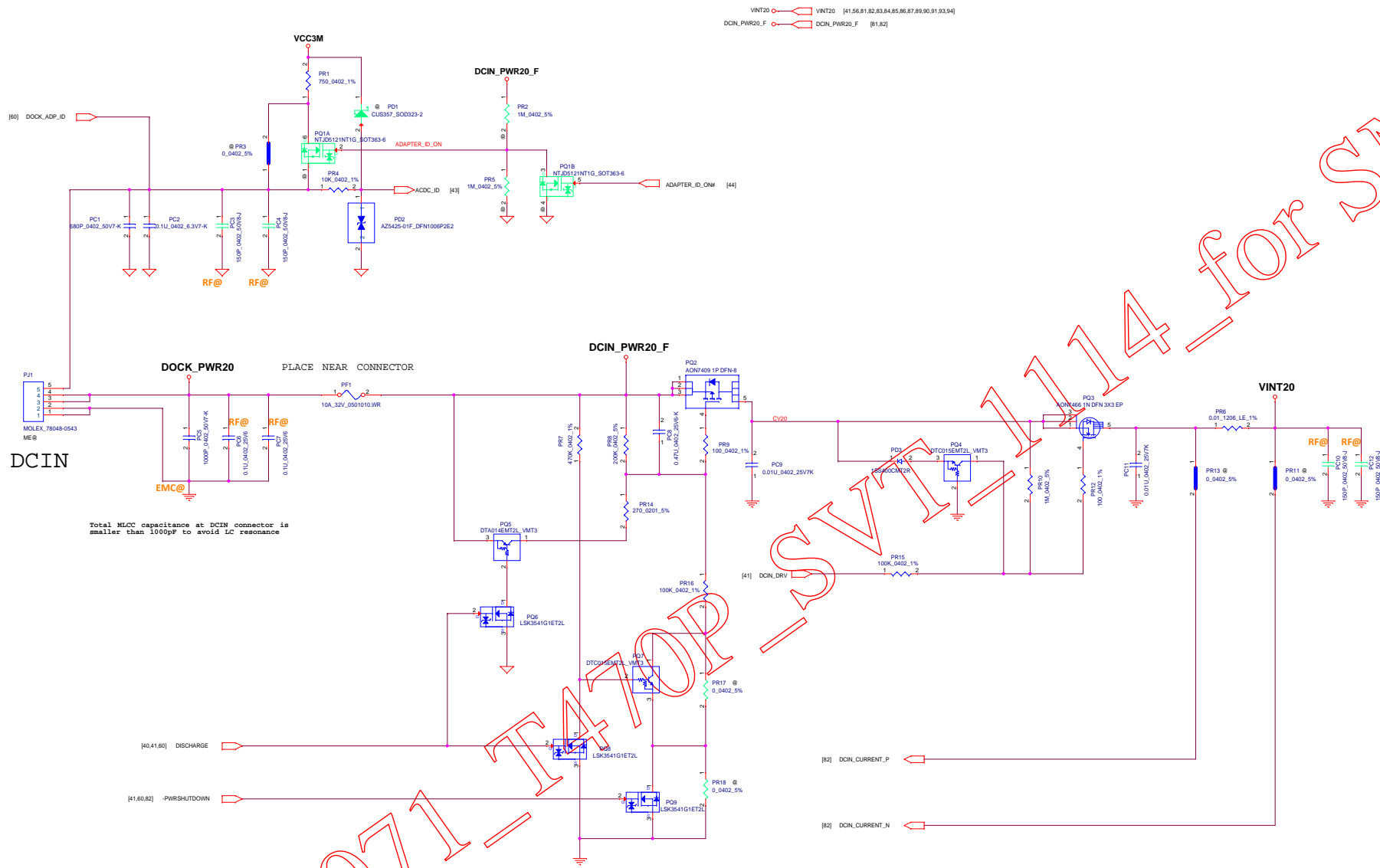


For ME hole

PCB Fedical Mark PAD



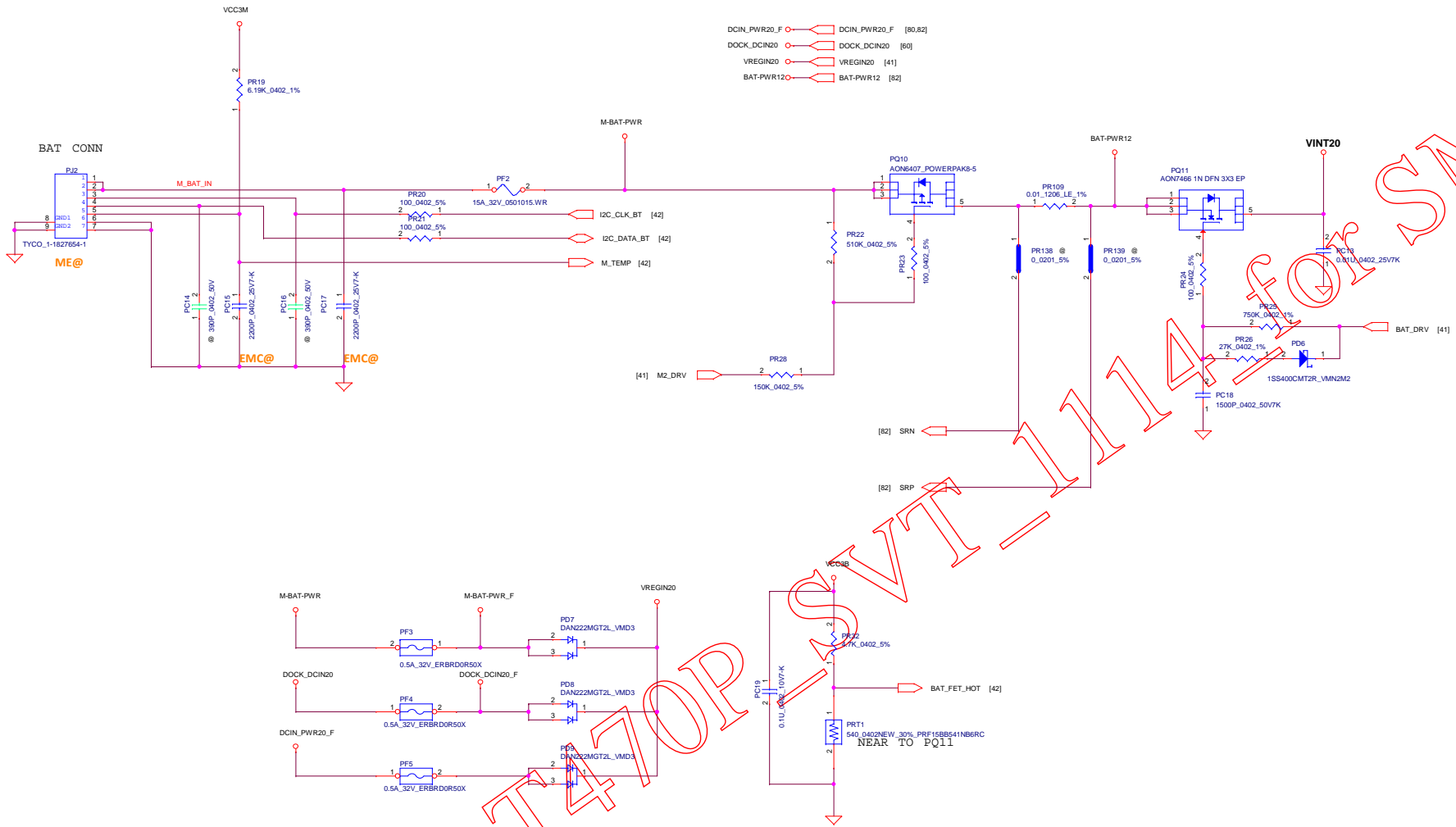
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Issued Date	2013/11/04	Deciphered Date	2014/12/31				
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TABLE

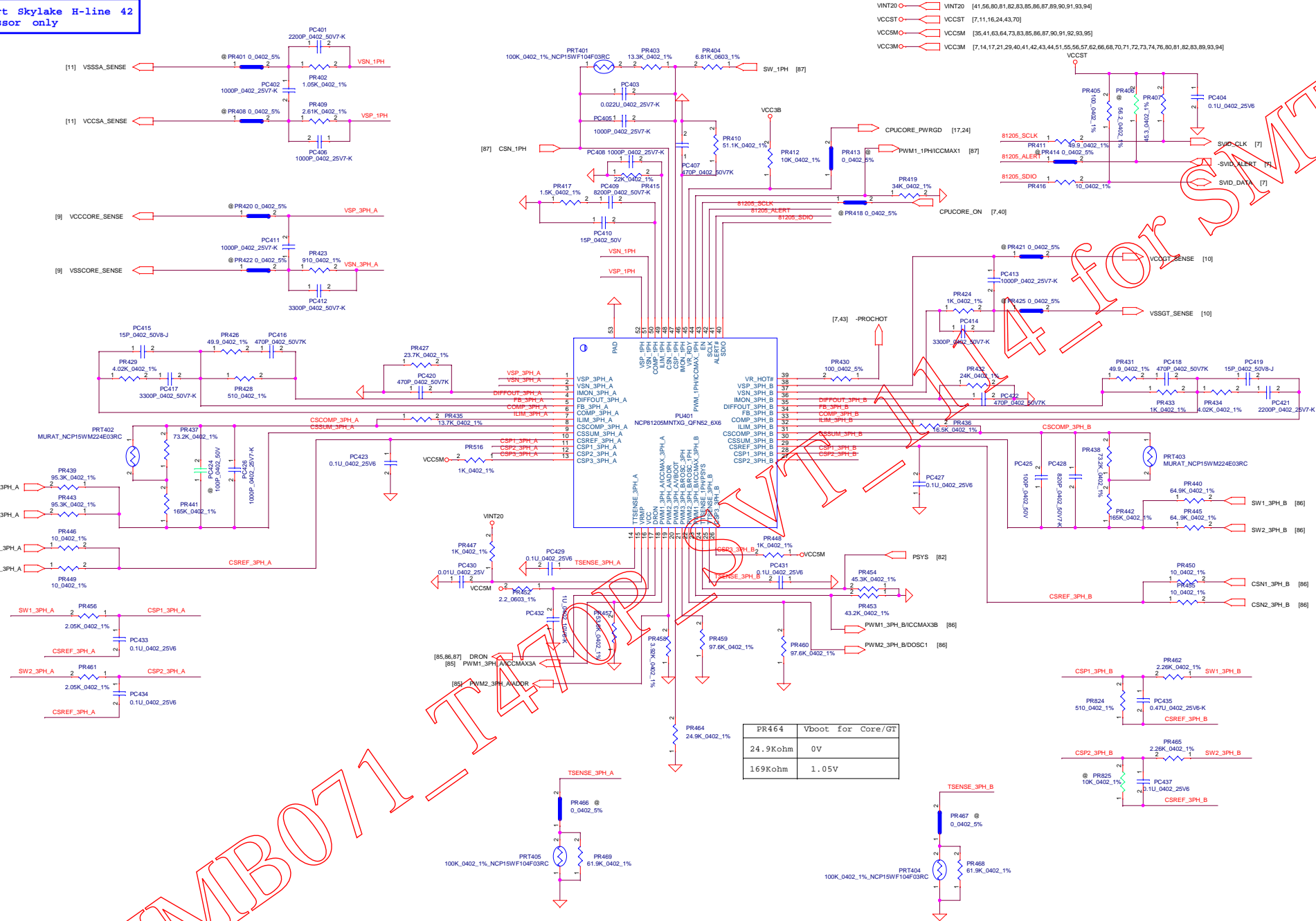
PEAK SHIFT	YES	NO
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PR7	ASM	NO-ASM
PQ8	ASM	NO-ASM
PQ7	ASM	NO-ASM

↑
LOGIC



NMB071-T470P

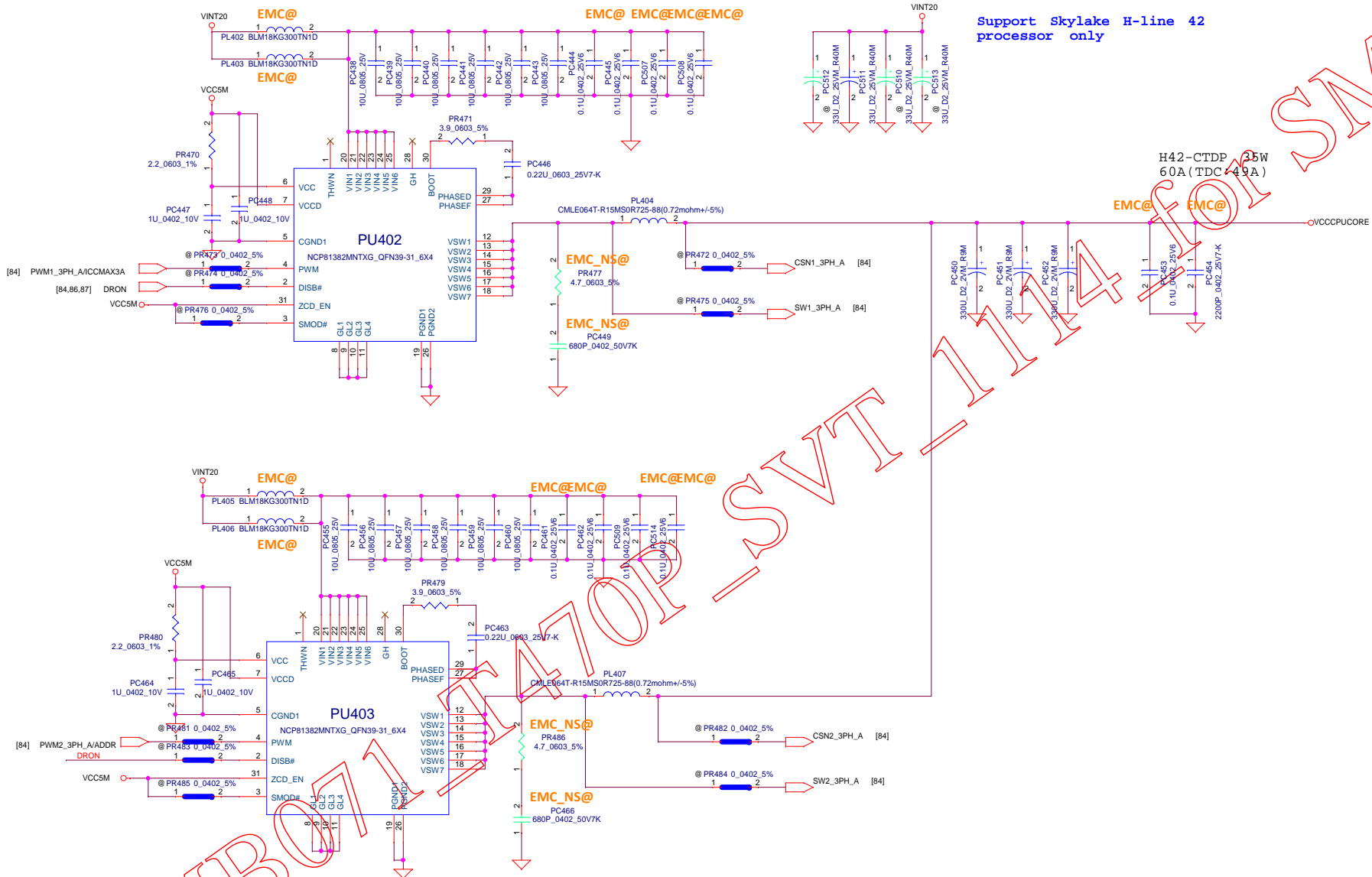
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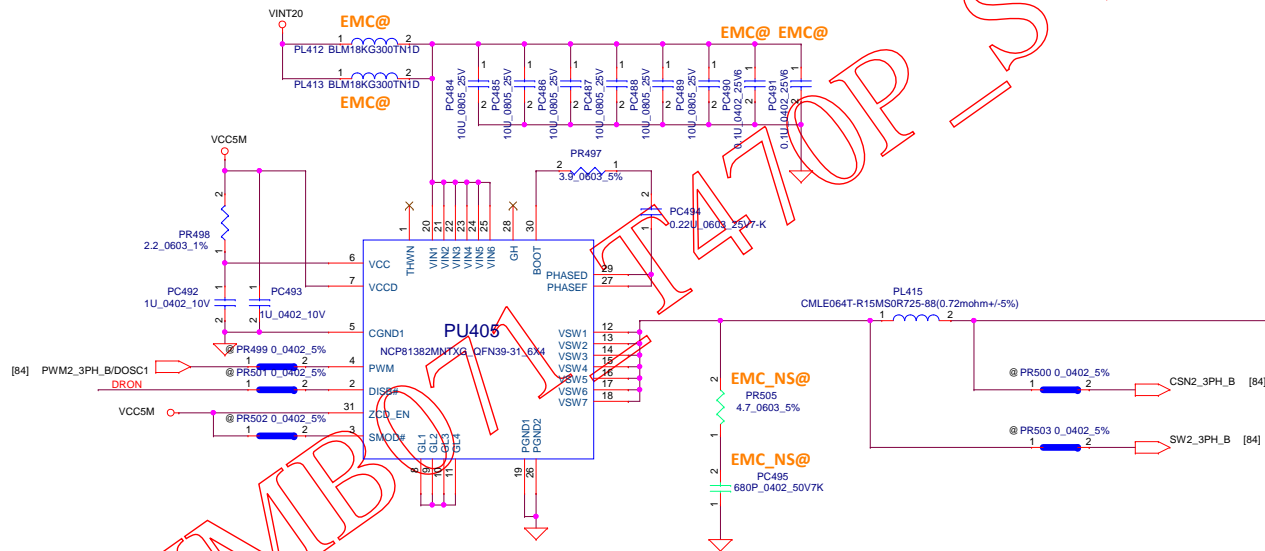
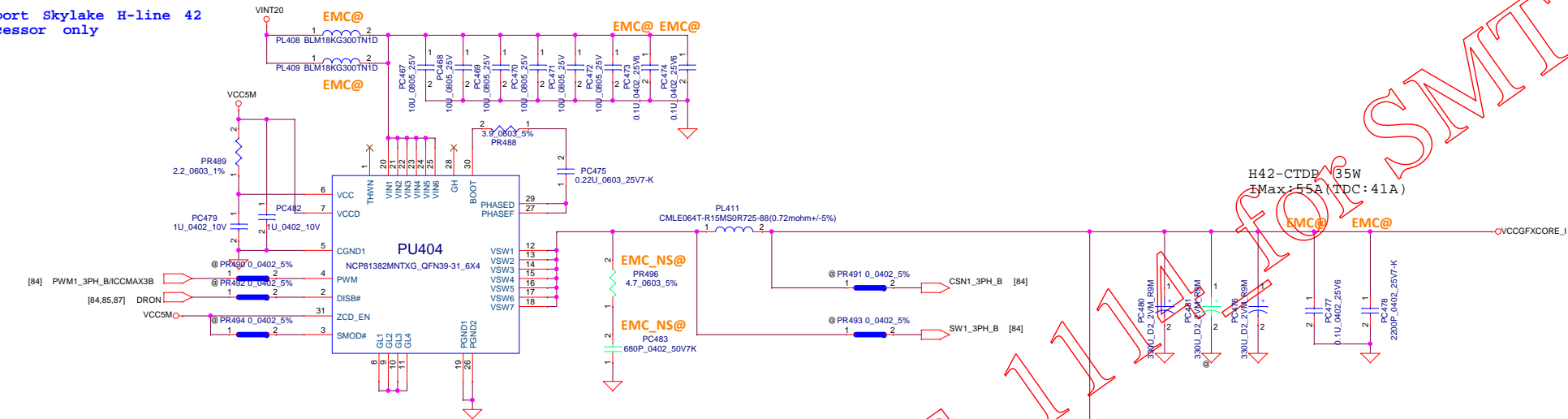
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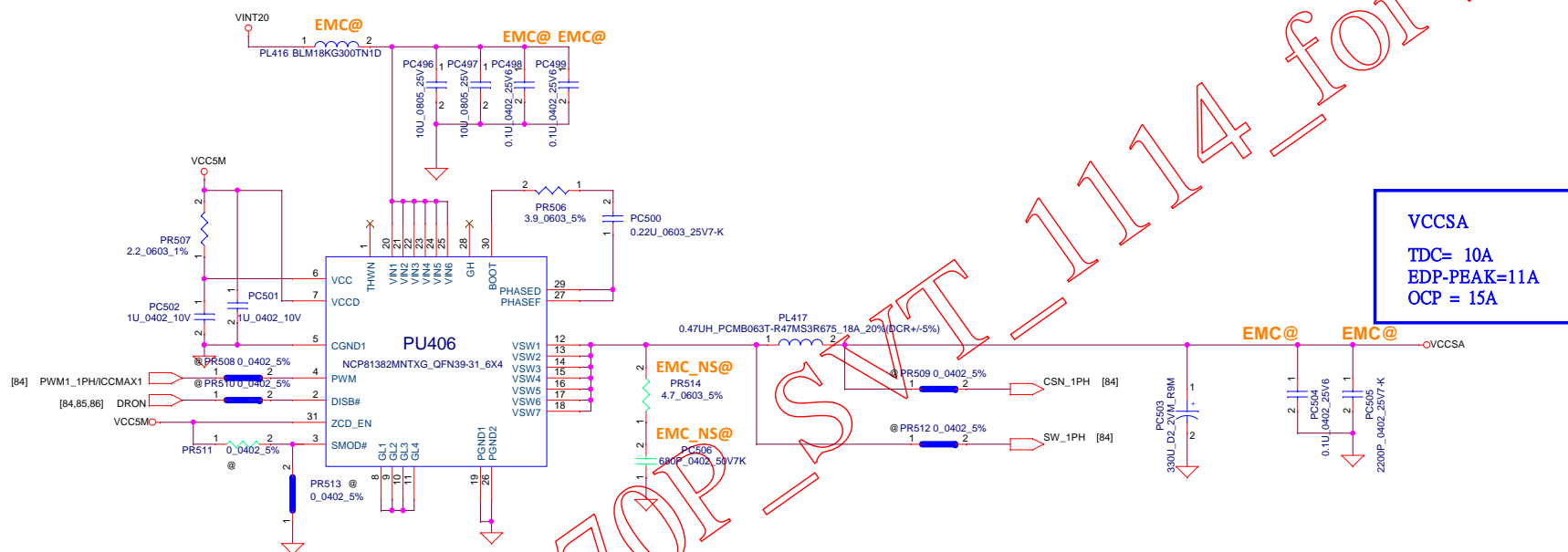
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						NW-A611 Rev 0.1	

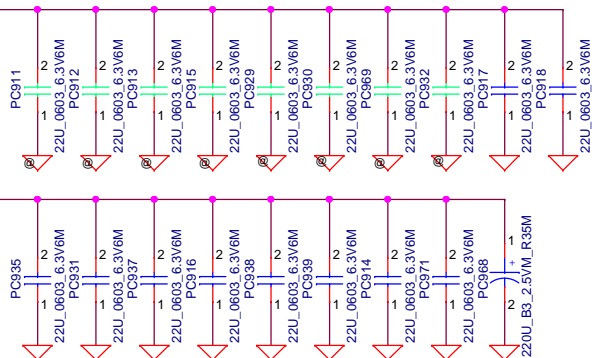
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				Sheet 87 of 99		

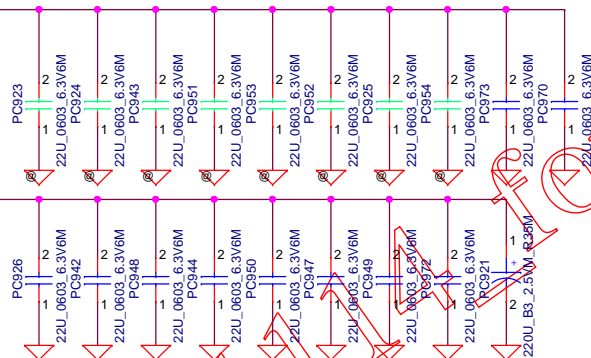
VCCCPUCORE

VCCCPUCORE
22uF 10pcs + 220uF/3528 1pcs



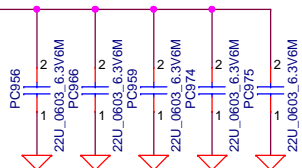
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VCCGFXCORE_I
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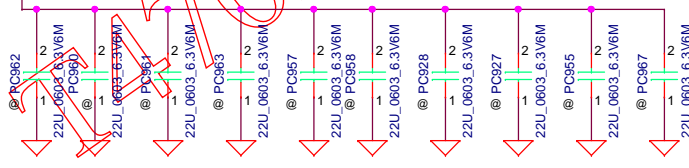


VCCSA

VCCSA
22uF 5pcs

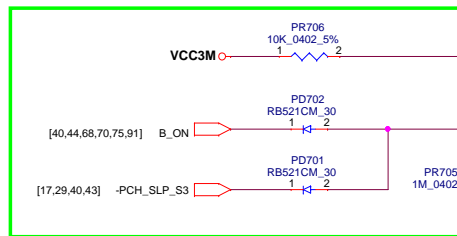


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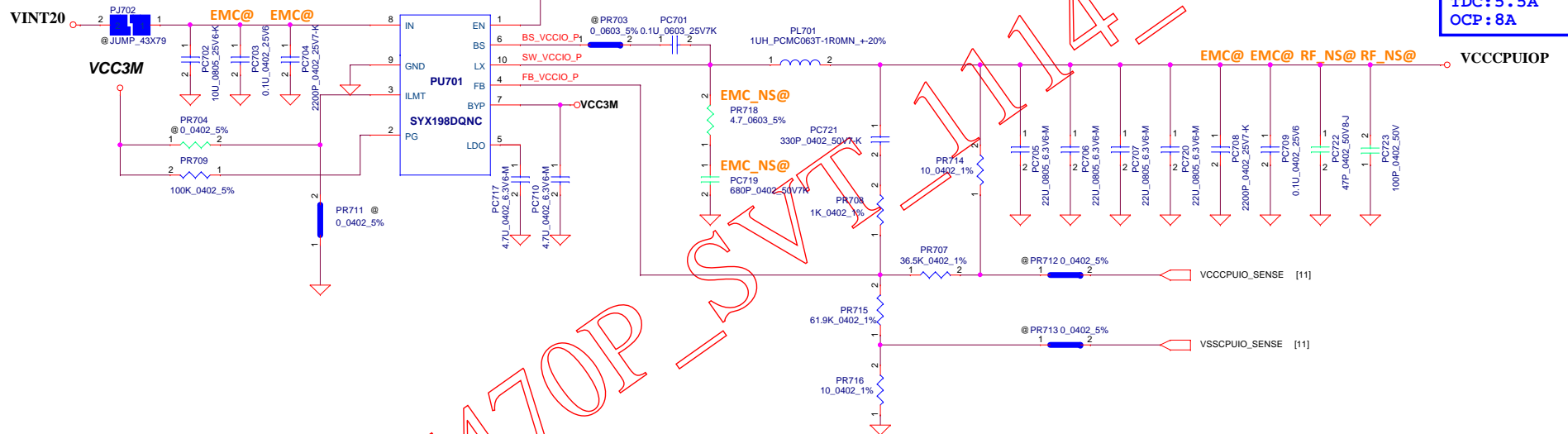


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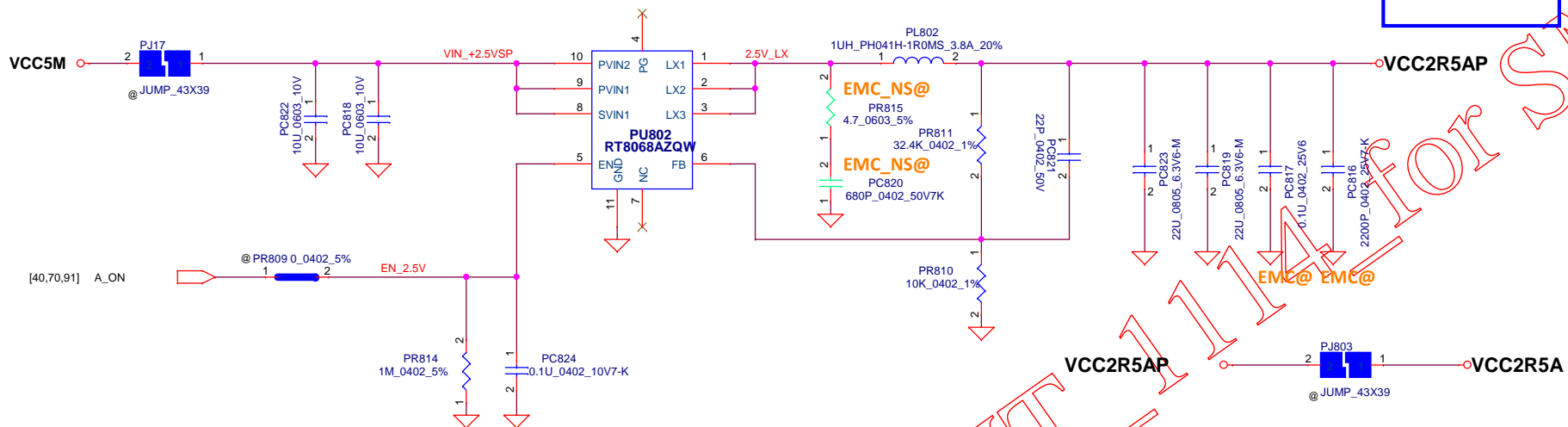


Follow Walter



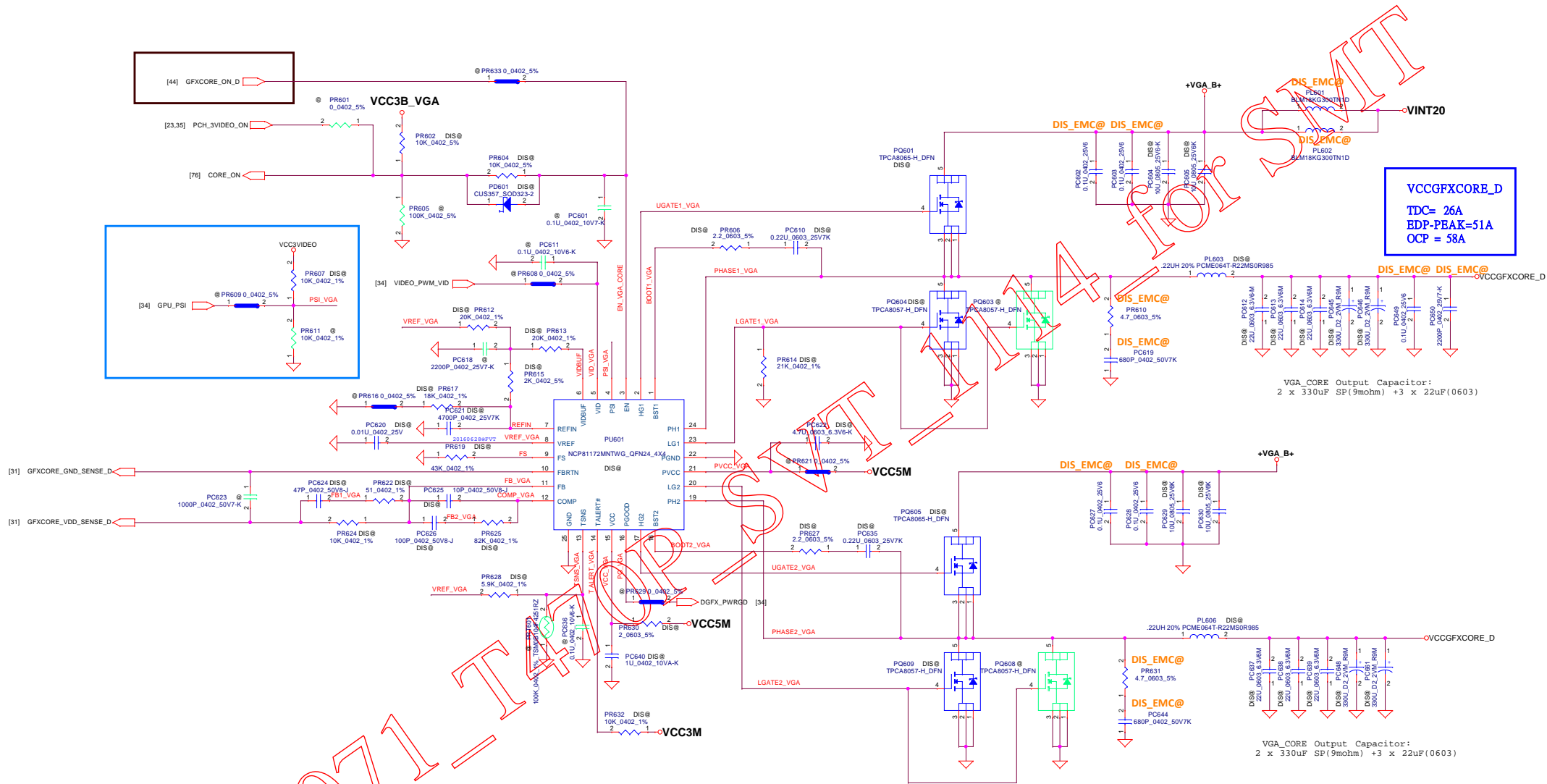
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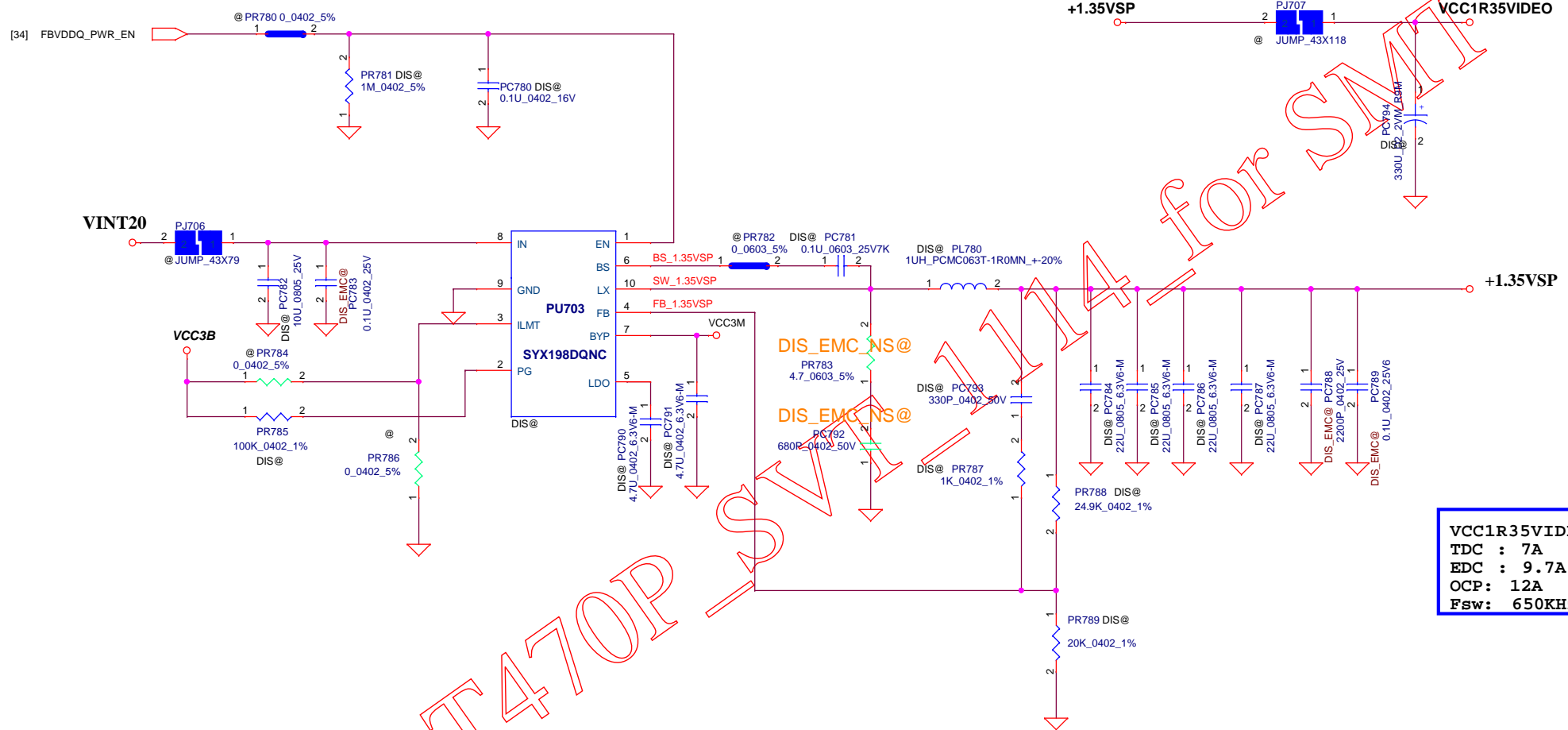
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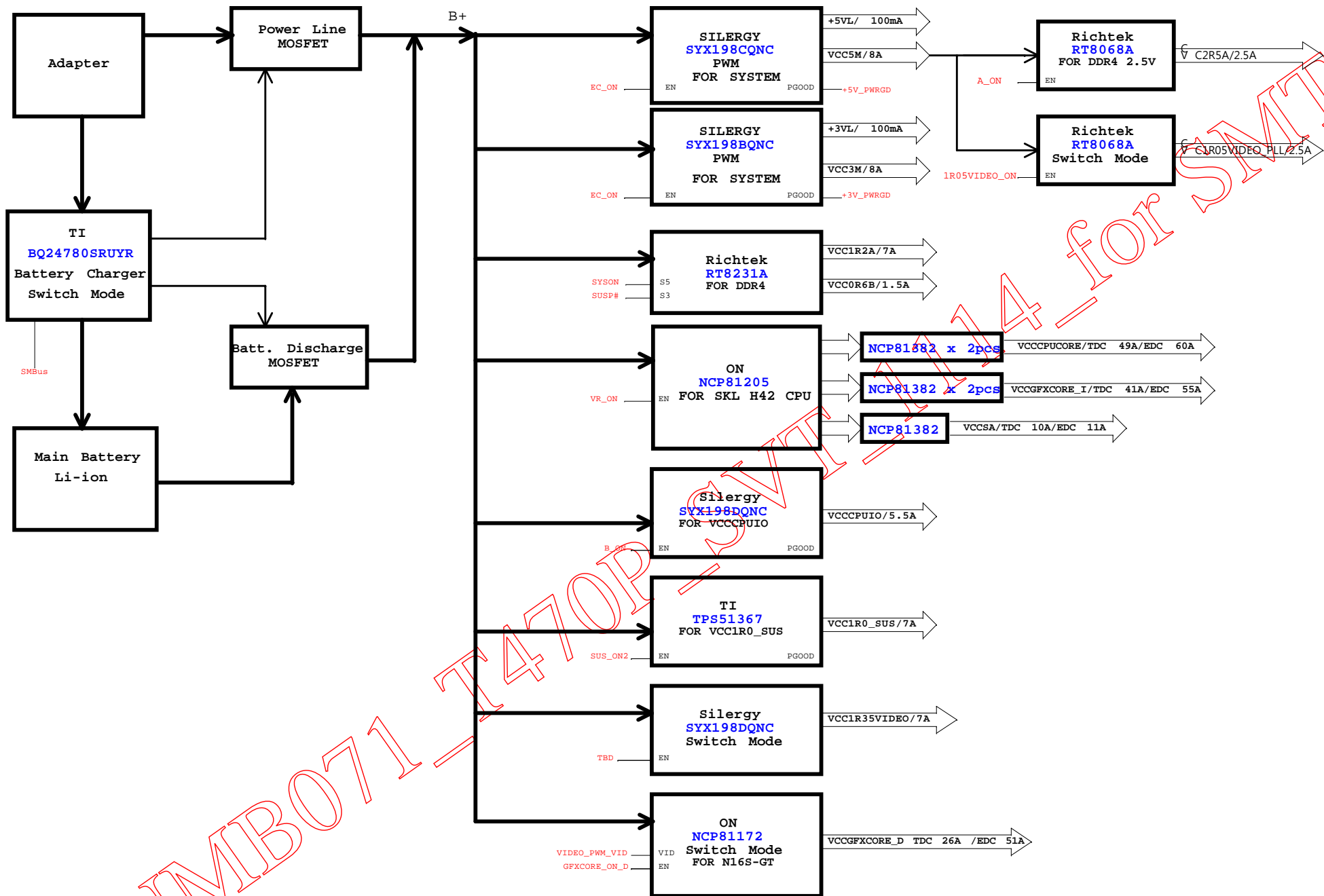


+0.6VSP		+0.6VSP [91]	VINT20		VINT20 [41,56,80,81,82,83,84,85,86,87,89,90,91,93,94]	VCCGFXCORE_D		VCCGFXCORE_D [31,35,76,93]	VCC3_SUS_SPI		VCC3_SUS_SPI [19,26,55]
+1.05VS_VGAP		+1.05VS_VGAP [95]	+3VL		+3VL [45,47,57,67,83]	VCC3VIDEO		VCC3VIDEO [31,34,35,93,95]	VCC5B_AVDD		VCC5B_AVDD [45]
+1.2VP		+1.2VP [91]	+5VL		+5VL [40,83]	VCC3B_VGA		VCC3B_VGA [34,35,76,93,95]	VCC5B_PVDD12		VCC5B_PVDD12 [45]
+1.35VSP		+1.35VSP [94]	VCC3M		VCC3M [7,14,17,21,29,40,41,42,43,44,51,55,56,57,62,66,68,70,71,72,73,74,76,80,81,82,83,89,93,94]	VCC1R05VIDEO		VCC1R05VIDEO [31,33,34,76,93]	VCC3_SUS_DVDDIO		VCC3_SUS_DVDDIO [45]
+V1.00AP		+V1.00AP [90]	VCC3_SUS		VCC3_SUS [7,14,15,16,17,18,21,23,24,26,29,42,43,45,62,71]	VCC1R5B_HDMI		VCC1R5B_HDMI [57,75]			
BAT-PWR12		BAT-PWR12 [81,82]	VCC3B		VCC3B [7,16,17,18,19,20,21,23,24,27,28,35,40,41,42,43,44,45,47,49,54,55,56,57,58,59,60,61,62,67,68,71,73,74,75,81,84,90,91,93,94]	VCC1R5HDMI		VCC1R5HDMI [75]	VCC3B_DVDD		VCC3B_DVDD [45]
DCIN_PWR20_F		DCIN_PWR20_F [80,81,82]	VCC5M		VCC5M [35,41,63,64,73,83,84,85,86,87,90,91,92,93,95]	VCC1R8CODEC		VCC1R8CODEC [75]			
DOCK_DCIN20		DOCK_DCIN20 [60,81]	VCC5B		VCC5B [41,45,57,59,61,65,66,67,71,73,75]	VCC1R8B_Codec		VCC1R8B_Codec [45,75]	VCC3B_MINIDP		VCC3B_MINIDP [59]
DOCK_DCIN20_F		DOCK_DCIN20_F [81]	VCCCPUCORE		VCCCPUCORE [9,85,88]				VCC3GBE		VCC3GBE [51,52,53]
DOCK_PWR20		DOCK_PWR20 [60,80]	VCCGFXCORE_I		VCCGFXCORE_I [10,86,88]				VCC3LAN		VCC3LAN [51,72]
M-BAT-PWR		M-BAT-PWR [81]	VCCSA		VCCSA [11,87,88]				VCC3M_EC		VCC3M_EC [43,44]
M-BAT-PWR_F		M-BAT-PWR_F [81]	VCCST		VCCST [7,11,16,24,43,70,84]				VCC3WWAN		VCC3WWAN [62,74]
VCC2R5AP		VCC2R5AP [92]	VCCSTG		VCCSTG [7,11,43,70]				VCC3WLAN		VCC3WLAN [62,74]
VCC3P		VCC3P [56]	VCCCPUIO		VCCCPUIO [5,6,11,89]				VCC5_TP		VCC5_TP [66,71]
VTTREF_0.6V		VTTREF_0.6V [91]	RTCVCC		RTCVCC [14,21,25,45]				VCC3_MC		VCC3_MC [54]
			VCC0R6B		VCC0R6B [27,28,91]						
			VCC3SW		VCC3SW [25,40,41,42,43,44,45,47,60,62,82]				+UIM_PWR		+UIM_PWR [62]
			VCC1R2A		VCC1R2A [7,11,17,27,28,91]				+USB_VCCA		+USB_VCCA [63]
			VCC1R35VIDEO		VCC1R35VIDEO [33,34,35,37,76,94]						
			VCC2R5A		VCC2R5A [27,28,75,92]						
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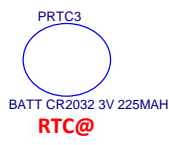
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3:10 OHM ALREADY CHANGE 470 OHM
RV3465,R7604,R7608

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LPX-Series

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